1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

J92 MLB NEWARK - DVT

11/21/2014

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ALIASES RESOLVED

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00107	1	SCHEM,MLB-NEWARK,J92	SCH	CRITICAL	
820-00045	1	PCBF,MLB-NEWARK,J92	PCB	CRITICAL	

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BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,CCSAK,MLB_MISC,MLB_DEBUG:ENG,MLB_PROGPARTS,EQ:4CH
MLB_MISC	CAM_FREQ:24M,CAM_XTAL:NO,EDP,RSMRST:SMC,PGOOD8:SLP_S4,SSD_LPSR:S3
MLB_DEBUG:ENG	XDP_CONN,XDP,HPMBB:SSP0,HPMVBUS:VDET
MLB_DEBUG:PVT	XDP_CONN,XDP,HPMBB:SSP0,HPMVBUS:VDET
MLB_DEBUG:PROD	XDP

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CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DRAM:HYN_2GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_2GB
DRAM:HYN_4GB_QDP	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB_QDP
DRAM:HYN_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:HYNIX_4GB
DRAM:HYN_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:H,DRAM_TYPE:HYNIX_8GB
DRAM:ELP_2GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_2GB
DRAM:ELP_4GB_QDP	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB_QDP
DRAM:ELP_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:ELPIDA_4GB
DRAM:ELP_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:H,DRAM_TYPE:ELPIDA_8GB

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 3	CFG 2
2GB	0	0
4GB QDP	0	1
4GB DDP	1	0
8GB	1	1

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00074	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NXP alt for Diodes dual
376S1089	376S1128		ALL	NXP alt for Diodes single
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
128S0393	128S0334		ALL	Kemet alt to Sanyo
372S0186	372S0185		ALL	NXP alt to Diodes
376S1053	376S0604		ALL	Diodes alt to Fairchild
197S0590	197S0588		ALL	Epson alt to TXC
197S0591	197S0588		ALL	NDK alt to TXC
107S0249	107S0251		ALL	TFT alt to Cyntec
138S0789	138S0941		ALL	Samsung alt to Murata
333S0700	333S0704		ALL	Hynix CAM DRAM alt to Elpida
333S00016	333S0704		ALL	Elpida new die CAM DRAM alt
333S00030	333S0704		ALL	Hynix new die CAM DRAM alt
339S0243	339S0244		ALL	Elpida SSD DRAM alt to Hynix
335S0948	335S0966		ALL	Winbond alt to Macronix
128S0631	128S0351		ALL	NEC alt to Sanyo
128S00008	128S0380		ALL	NEC alt to Sanyo
311S00007	311S0426		ALL	Sanyo alt to NEC
311S00008	311S0271		ALL	Samsung alt to Murata
311S00018	311S0409		ALL	Diodes alt to NXP
740S00004	740S0134		ALL	Kemet alt to Sanyo
740S00005	740S0190		ALL	Polytronics alt to Wayon
128S0296	128S0487		ALL	Sanyo alt to NEC
128S00012	128S0487		ALL	ROHM alt to NEC
128S00025	128S0469		ALL	Kemet alt to Sanyo
128S0374	128S0469		ALL	NEC alt to Sanyo
376S00007	376S1179		ALL	AOS alt to Vishay
376S1080	376S0820		ALL	Diodes alt to OnSemi
376S00036	376S1194		ALL	Vishay alt to OnSemi
376S00037	376S1193		ALL	Vishay alt to OnSemi
685-00004	685-00003	SSDRAM:A1_ELP	ALL	Hynix SSD DRAM alt to Elpida
337S00061	337S00054	CPU:0.8GHZ	ALL	2.4G turbo CPU alt to 2.0G

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4638	1	IC,MCU,LPC11U37,128KB/12KB,TFBGA48	U4600	CRITICAL	HPM:BLANK
341S00190	1	IC,HPM (VXXX) DVT,X261	U4600	CRITICAL	HPM:PROG
338S1231	1	IC,SMC12-B1,40MHZ/50DMIPS MCU,7X7,168BGA	U5000	CRITICAL	SMC:BLANK
341S00031	1	IC,SMC-B1,EXTERNAL (VXXXX) PROTO2A, J92	U5000	CRITICAL	SMC:PROG
335S1009	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_WIN:BLANK
335S1010	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_MAC:BLANK
335S1029	1	64 MBIT SPI QUAD I/O FLASH,CSP,3.3V,QUAD IO	U6100	CRITICAL	BOOTROM_MIC:BLANK
341S00191	1	EFI ROM,MLB (VXXX) DVT,X261	U6100	CRITICAL	BOOTROM:PROG
335S0948	1	IC,SPI SERIAL FLASH,64M BITS,1.8V,WLBGA	U8800	CRITICAL	SSDROM_WIN:BLANK
335S0966	1	IC,SPI SERIAL FLASH,64M BITS,1.8V,WLCSP	U8800	CRITICAL	SSDROM_MAC:BLANK
341S00091	1	S1-X SSD BOOTROM, UI64	U8800	CRITICAL	SSDROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00054	1	IC,CPU,BW,Q6KZ,Q5,E0,2/2,0.8,4.5W,.8,B1234	U0500	CRITICAL	CPU:0.8GHZ
337S00099	1	IC,CPU,BW,QH2Z,PRQ,F0,2/2,1.1,5W,.85,B1234	U0500	CRITICAL	CPU:1.1GHZ
337S00098	1	IC,CPU,BW,QH2V,PRQ,F0,2/2,1.2,5W,.9,B1234	U0500	CRITICAL	CPU:1.2GHZ
337S00097	1	IC,CPU,BW,QH2R,PRQ,F0,2/2,1.3,5W,.9,B1234	U0500	CRITICAL	CPU:1.3GHZ
946-3892	1	J11/J13 MLB DYMAX ADHESIVE 29993-SC 0.4G	GLUE	CRITICAL	
825-7995	1	LABEL,BARCODE,2D,1D,CONFIG,MLB,X261	LABEL		

SSD POP Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S0243	1	POP,S1-X CONTROLLER+4GBITS ELP,841B,FCBGA	U8400	CRITICAL	SSDRAM:A0_ELP
339S0244	1	POP,S1-X CONTROLLER+4GBITS HYN,841B,FCBGA	U8400	CRITICAL	SSDRAM:A0_HYN
685-00003	1	POP,MLB,S1X-A1,ELP-4GBIT,X261	U8400	CRITICAL	SSDRAM:A1_ELP
685-00004	1	POP,MLB,S1X-A1,HYN-4GBIT,X261	U8400	CRITICAL	SSDRAM:A1_HYN
338S1288	1	IC,S1-X,CONTROLLER,A1,841(312)B,FCCSP	SSD_CTRL	CRITICAL	S1X:A1
338S00055	1	IC,S1-X,CONTROLLER,A2,841(312)B,FCBGA	SSD_CTRL	CRITICAL	S1X:A2
333S0733	1	IC,LPDDR2,128MX32,1.2V,ELPIDA 28NM,312B	SSD_DRAM	CRITICAL	S1X_DRAM:ELPIDA
333S0694	1	IC,LPDDR2,128MX32,1.2V,HYNIX 29NM,312B	SSD_DRAM	CRITICAL	S1X_DRAM:HYNIX
870-00878	1	TAPE,CONDUCTIVE,SSD,REEL,X261	SSD_TAPE	CRITICAL	

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-6486	2	IC,SDRAM,LPDDR-1600,8GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_2GB
333S00028	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_4GB_QDP
998-6453	2	IC,SDRAM,LPDDR-1600,8GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_2GB
998-6454	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_4GB_QDP
333S0730	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0731	2	IC,SDRAM,LPDDR-1600,32GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0740	2	IC,SDRAM,LPDDR-1600,16GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0741	2	IC,SDRAM,LPDDR-1600,32GBIT,253B FBGA	U2300,U2500	CRITICAL	DRAM_TYPE:ELPIDA_8GB

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BOM Configuration

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Top level BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-6568	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6569	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6570	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6571	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6572	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6573	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6574	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6575	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6576	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6577	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6578	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6579	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP
639-6580	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6581	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6582	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6583	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6584	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6585	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6586	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6587	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6588	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6589	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6590	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6591	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP
639-6592	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6593	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6594	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6595	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6596	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6597	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6598	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6599	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6600	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6601	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6602	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6603	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP
639-6604	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6605	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6606	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6607	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6608	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6609	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6610	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6611	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6612	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6613	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6614	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP
639-6615	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP

Partial & development BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00014	CMN PTS,PCBA,MLB-NEWARK,J92	MLB_COMMON
685-00003	POP,MLB,S1X-A2,ELP-4GBIT,X261	S1X:A2,S1X_DRAM:ELPIDA
685-00004	POP,MLB,S1X-A2,HYN-4GBIT,X261	S1X:A2,S1X_DRAM:HYNIX
939-00043	PCBA,MLB,NO CPU,EL 8GB,TOSH 256G,WIFI FCC,X261	ALTERNATE,CMN,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP

Common BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00014	1	CMN PTS,PCBA,MLB-NEWARK,J92	CMNPTS	CRITICAL	CMN

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00196	1	BT ROM (VXX) DVT,2MBIT,X261	U3570	CRITICAL	BT:PROG
341S00197	1	WIFI ROM (PXXXX) DVT,WW1,X261	U3580	CRITICAL	WIFI:FCC
341S00198	1	WIFI ROM (PXXXX) DVT,WW2,X261	U3580	CRITICAL	WIFI:ETSI
341S00199	1	WIFI ROM (PXXXX) DVT,WW3,X261	U3580	CRITICAL	WIFI:APAC
341S00200	1	WIFI ROM (PXXXX) DVT,IND,X261	U3580	CRITICAL	WIFI:IND

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,BT:PROG,SMC:PROG,SSDROM:PROG,HPM:PROG

SYNC_MASTER=J43_MLB SYNC_DATE=10/24/2012

PAGE TITLE
J92 BOM Variants

Apple Inc.

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REVISION <E4LABEL>

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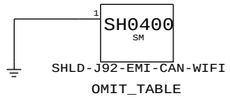
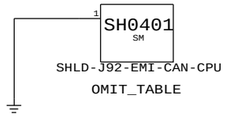
WIFI EMI CAN



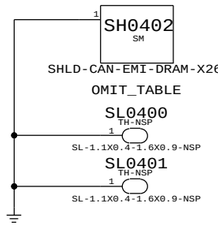
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-7064	1	CAN,EMI,WIFI,X261	SH0400	CRITICAL	

CPU EMI CAN



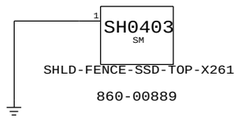
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-00112	1	CAN,EMI,CPU,X261	SH0401	CRITICAL	

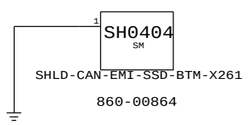
DRAM EMI CAN & SLOTs



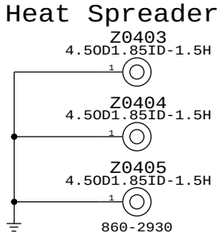
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-00400	1	CAN,EMI,DRAM,TALL,X261	SH0402	CRITICAL	

SSD EMI FENCE & CAN

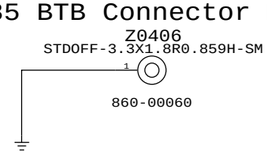




CPU Heat Spreader Bosses



E85 BTB Connector Boss



SYNC_MASTER=J43_MLB SYNC_DATE=10/24/2012

PAGE TITLE
PD PARTS

Apple Inc.

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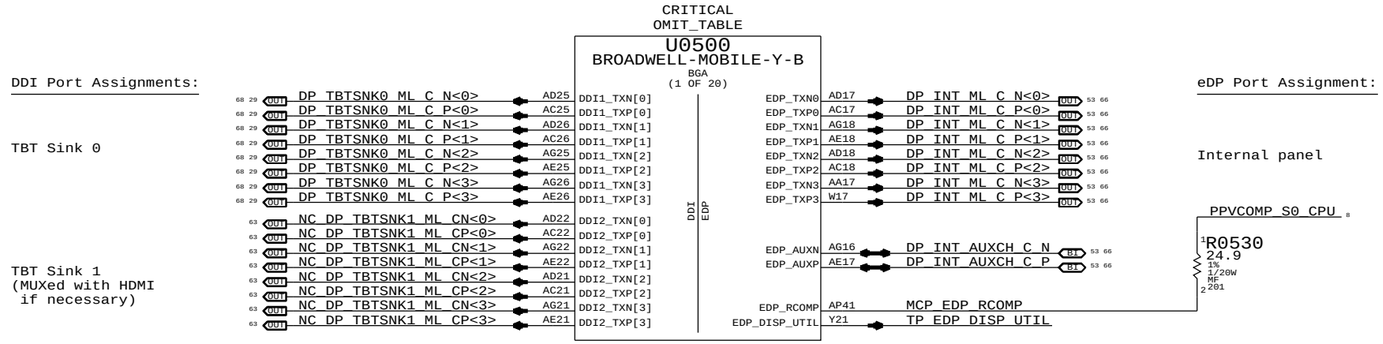

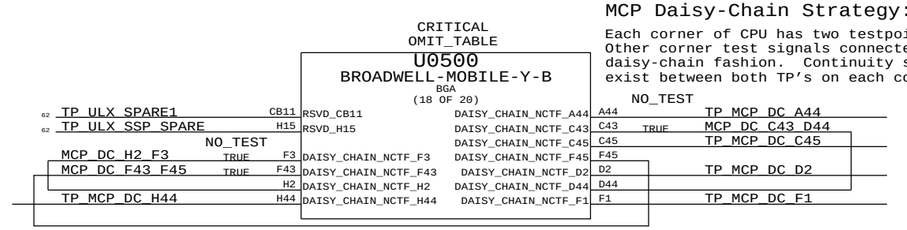

MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.

SYNC_MASTER=J92_WILL SYNC_DATE=04/10/2013

PAGE TITLE
CPU GFX/DC_TEST

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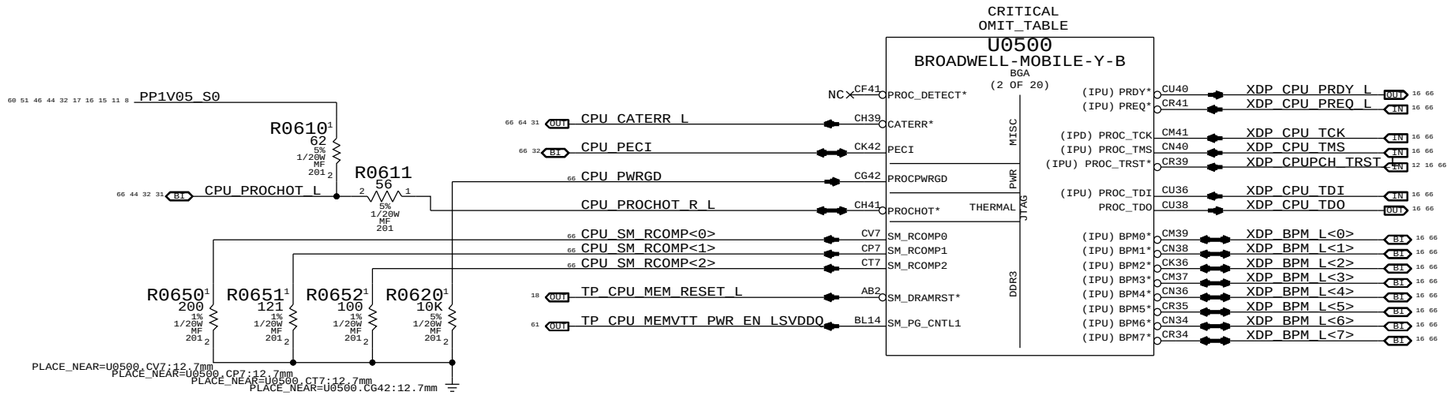
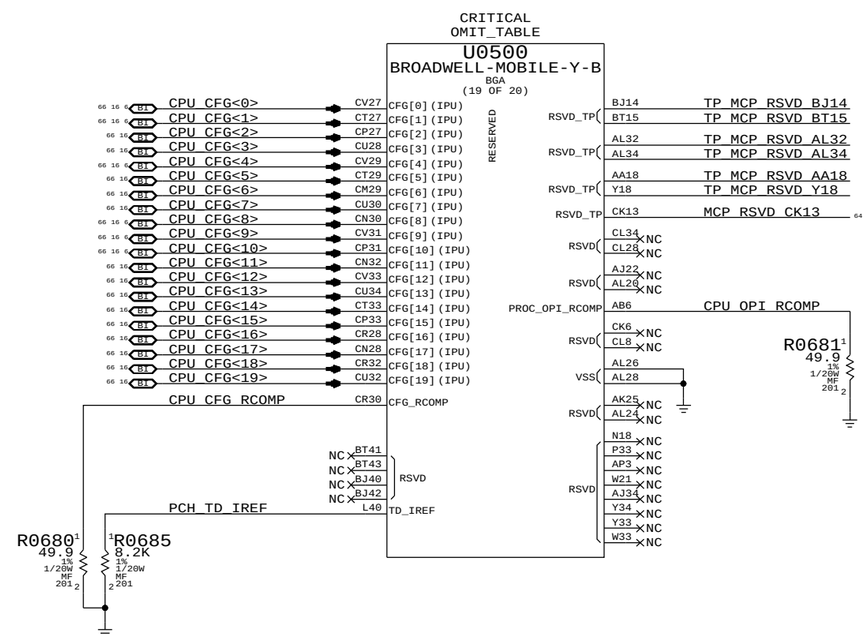
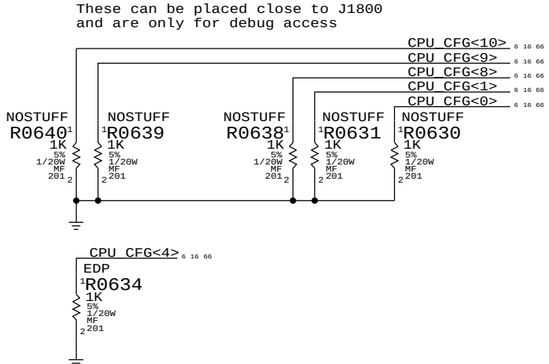




TBD: Confirm w/ Intel which still apply for BDW-Y

CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access



SYNC_MASTER=J92_WILL SYNC_DATE=04/10/2013

PAGE TITLE
CPU Misc/JTAG/CFG/RSVD

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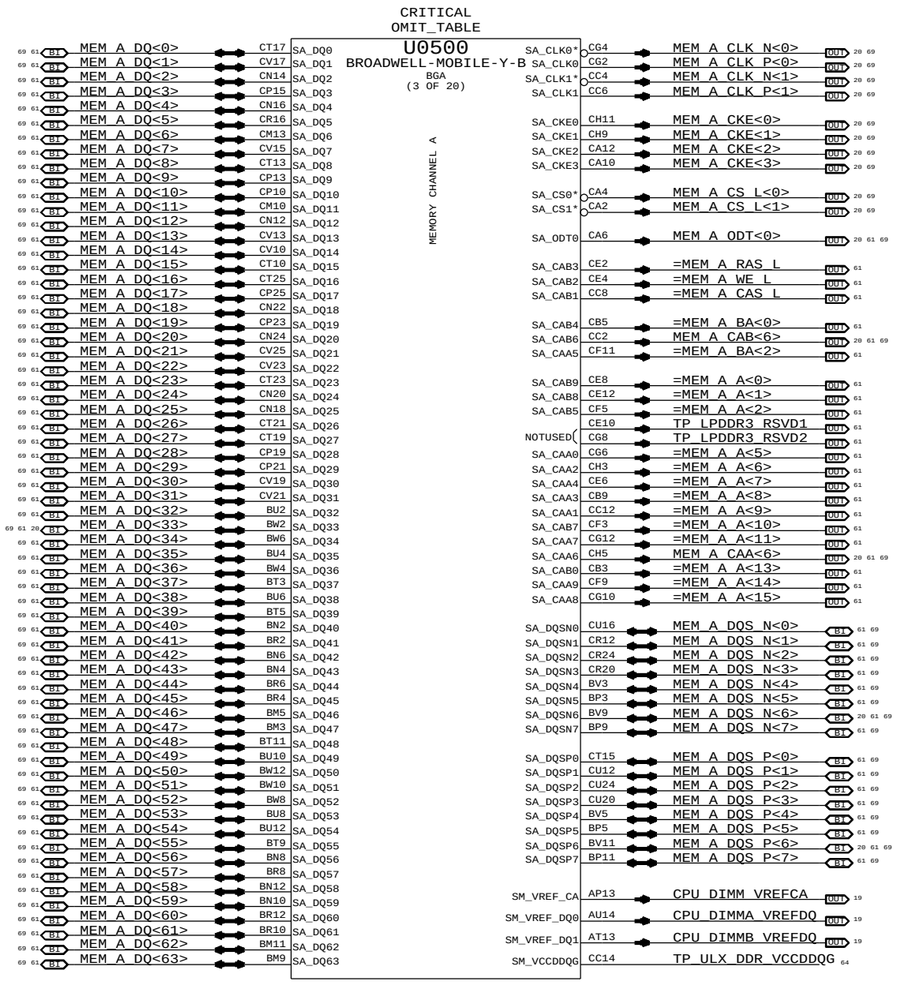

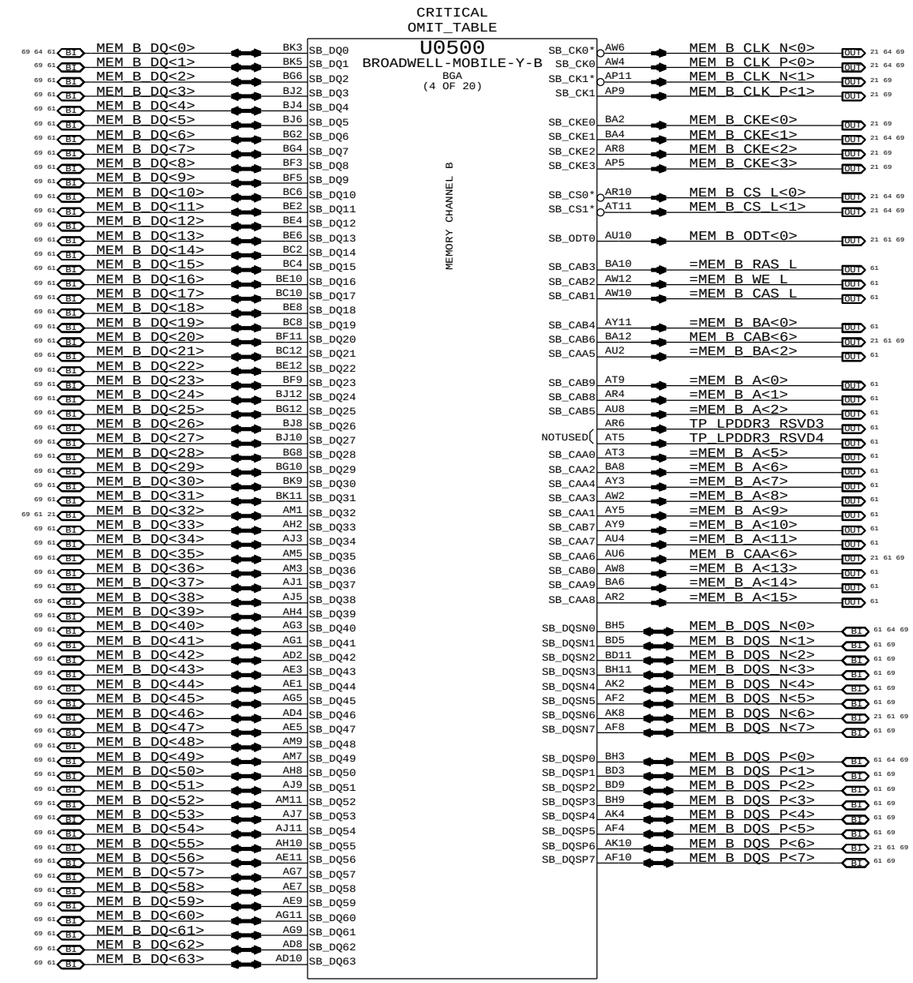

SYNC_MASTER=J92_LS_MLB SYNC_DATE=07/17/2013

PAGE TITLE
CPU DDR3/LPDDR3 Interfaces

Apple Inc.

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HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.

NOTE: Aliases not used on CPU supply outputs to avoid any extraneous connections.

CRITICAL
OMIT_TABLE
U0500
BROADWELL-MOBILE-Y-B
BGA
(12 OF 20)
BRW ULX POWER

1.4A Max (DDR3: 1.5-1.35V)
1.1A Max (LPDDR3: 1.2V)
PP1V2_S3

TP_MCP_DC_CY3
TP_MCP_DC_CW1

PPVCC_S0_CPU
R0860 100 5% 1/20W MF 201
PLACE_NEAR=U0500.CH45:50.8mm

CPU_VCCSENSE_P
TP_PPVCCIO_S0_CPU
Max load: 300mA
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
PPVCOMP_S0_CPU
Max load: 300mA
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

PP1V05_S0
R0800 75 1% 1/20W MF 201
R0802 130 1% 1/20W MF 201
R0810 43 5% 1/20W MF 201
R0811 0 5% 1/20W MF 0201
R0812 0 5% 1/20W MF 0201

CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT

R0802.2: PLACE_NEAR=U0500.CE40:2.54mm
R0810.2: PLACE_NEAR=U0500.CD43:38.1mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm

CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R
CPU_VCCST_PWRGD
CPU_VR_EN
CPU_VR_READY
R0850 10K 5% 1/20W MF 201
CPU_PWR_DEBUG_L
TP_MCP_RSVD_CJ22
TP_MCP_RSVD_CK23
TP_IVR_ERROR
TP_IST_TRIGGER

PPVCC_S0_CPU
32A Max
MCP_DC_CV45
TP_MCP_DC_CY44

CRITICAL
OMIT_TABLE
U0500
BROADWELL-MOBILE-Y-B
BGA
(13 OF 20)

PP1V05_S0SW_PCH_PCIE
PP1V05_S0SW_PCH_SATA
PP1V05_S0SW_PCH_USB3
PP1V05_S0
PP1V05_S0SW_PCH_VCCSATA3PLL
PP1V05_S0SW_PCH_VCCUSB3PLL
PP1V05_S0_PCH_VCCAPLL_OPI
PP1V05_SUS
PP1V5_S0
PP1V05_SUS
PP3V3_SUS
PP3V3_S5
PP3V3_S0
PP1V05_S0_PCH_VCC_ICC
PP1V05_S0_PCH_VCCACLKPLL
PP1V05_S0
PP3V3_SUS

PP3V3_SUS
PPVRTC_G3H
PPVOUT_S0_PCH_DCPRTC
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
C0892 0.1UF 10% 10V X5R-CERM 0201
C0891 0.1UF 10% 10V X5R-CERM 0201
C0890 1UF 20% 6.3V X5R 0201
BYPASS=U0500.AA15::6.35mm
C0895 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U0500.V15::6.35mm
PP1V05_S0
???mA Max

PP3V3_S5
C0897 0.47UF 10% 6.3V CERM-X5R 0201
PLACE_NEAR=U0500.AG13:6.35mm
R0896 0 5% 1/20W MF 0201
PP1V05_S5_PCH_VCCDSW
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
PP1V05_S5_PCH_VCCDSW_R
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.05V
C0896 1UF 20% 6.3V X5R 0201
BYPASS=U0500.AG13::6.35mm

RTC
SPI
HSIO
OPI
USB3
CORE
AZALIA/HDA
VRM/USB2/AZALIA
MISC
THERMAL SENSOR
GPIO/LCC
SERIAL IO
SUS OSCILLATOR
ICC
USB2
WPT LP POWER

SYNC_MASTER=J92_DEVMLB SYNC_DATE=10/01/2013
PAGE TITLE
CPU/PCH POWER
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SHEET 8 OF 75

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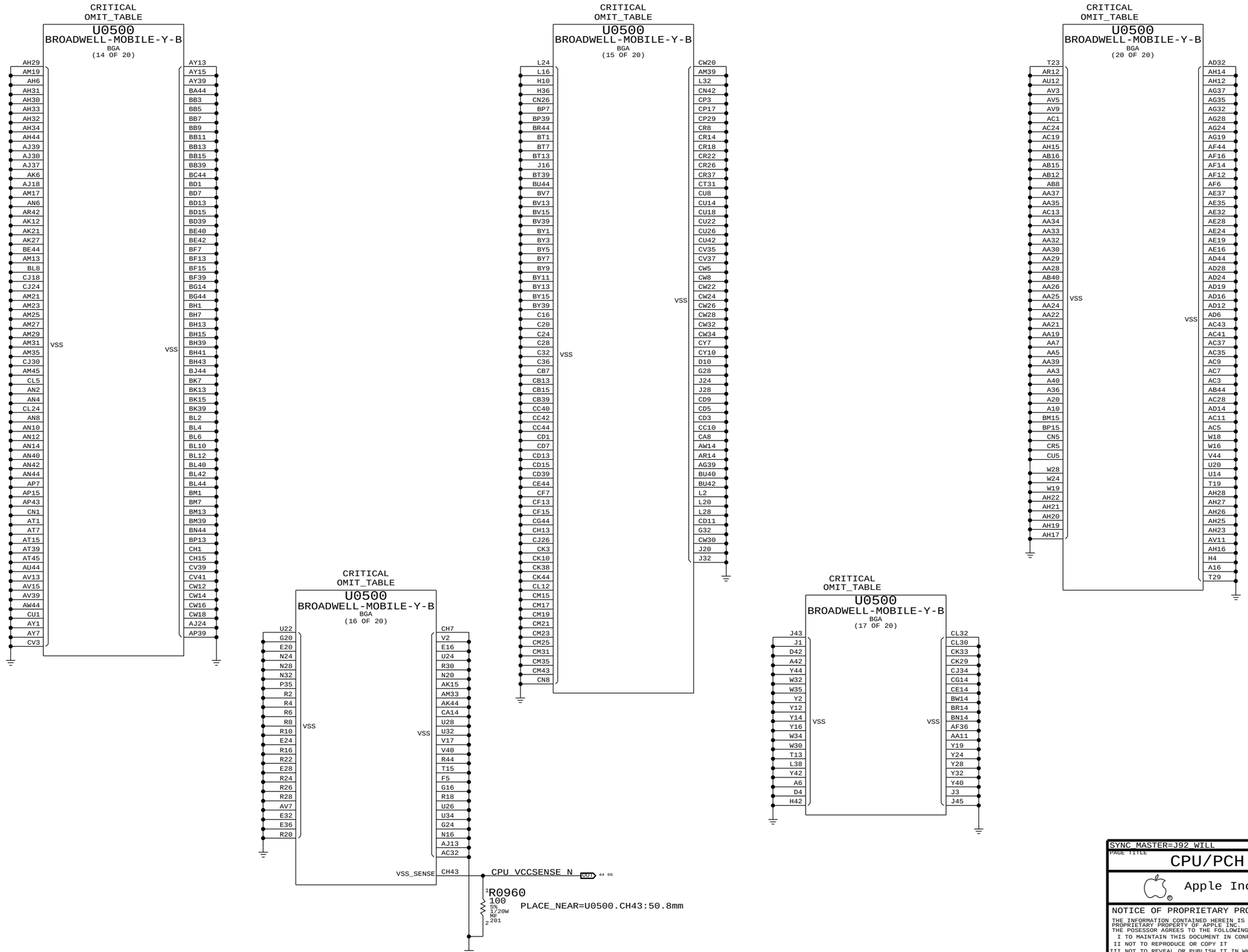

SYNC_MASTER=J92_WILL SYNC_DATE=04/10/2013

PAGE TITLE
CPU/PCH GROUNDS

Apple Inc.

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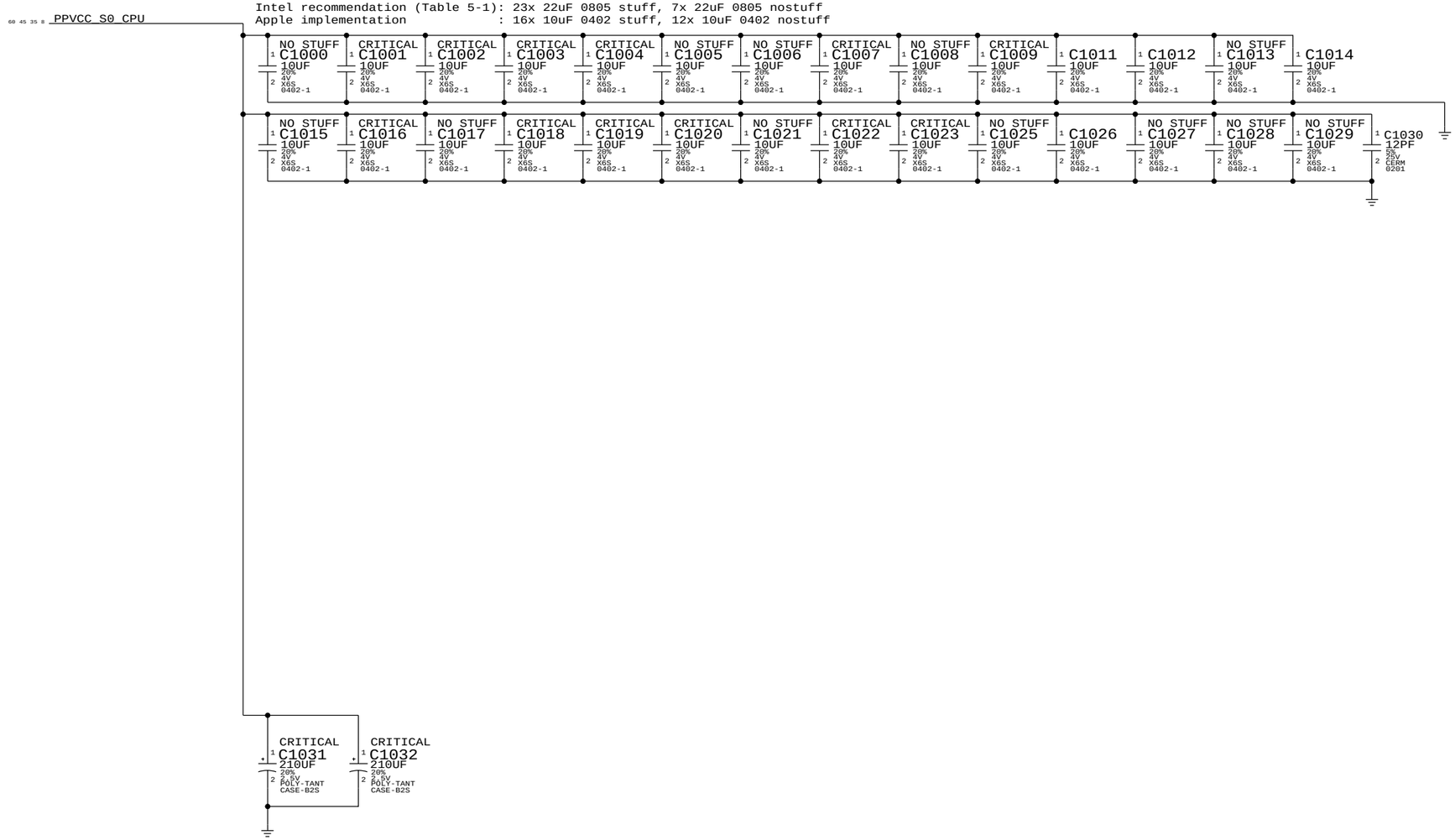
All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 0.9 unless stated otherwise

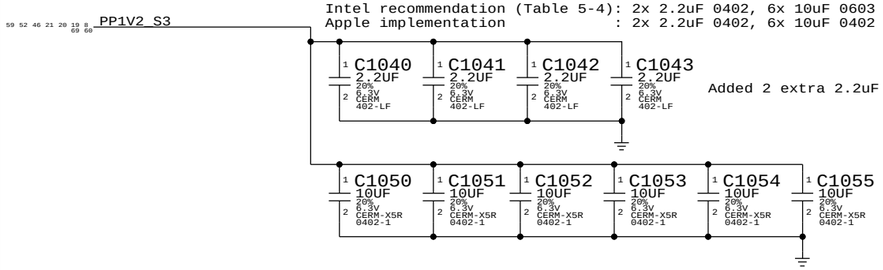
CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 16x 10uF 0402 stuff, 12x 10uF 0402 nostuff



CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 2x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 2x 2.2uF 0402, 6x 10uF 0402



Added 2 extra 2.2uF per Harris Beach v0.9 schematic

SYNC_MASTER=J92_DEVMLB SYNC_DATE=10/01/2013

PAGE TITLE: CPU Decoupling

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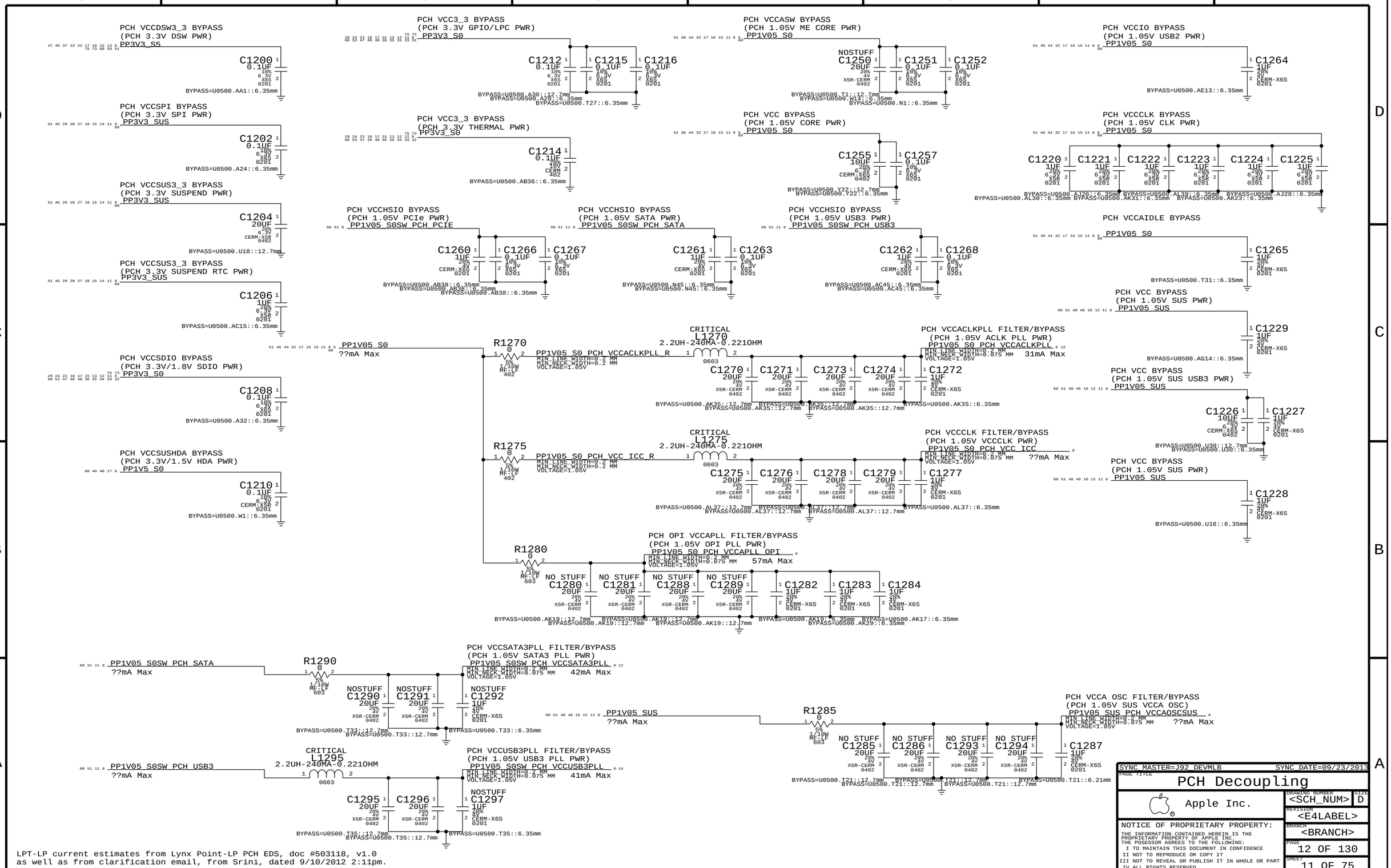

LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

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PAGE TITLE
PCH Decoupling

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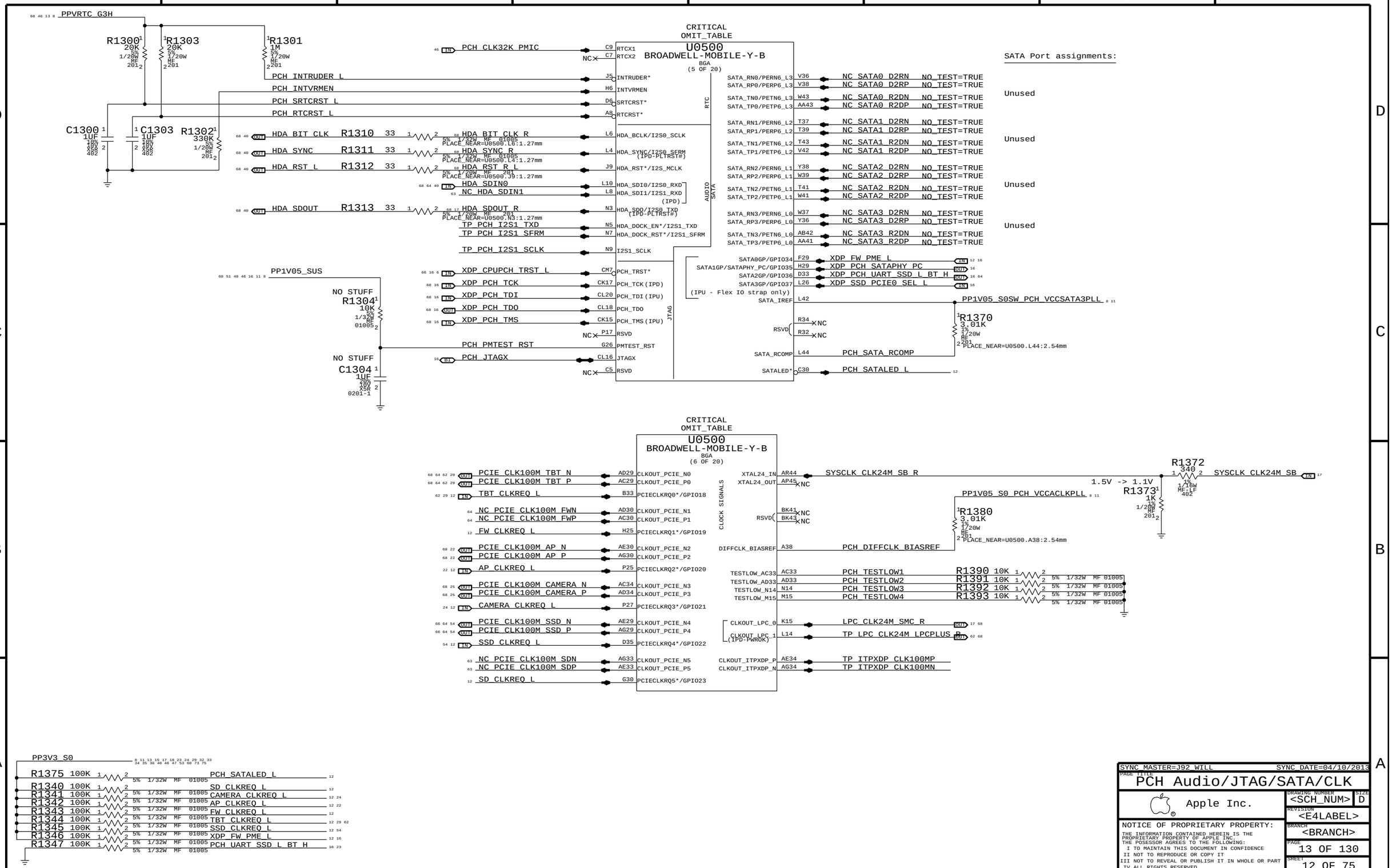

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PAGE TITLE: PCH Audio/JTAG/SATA/CLK

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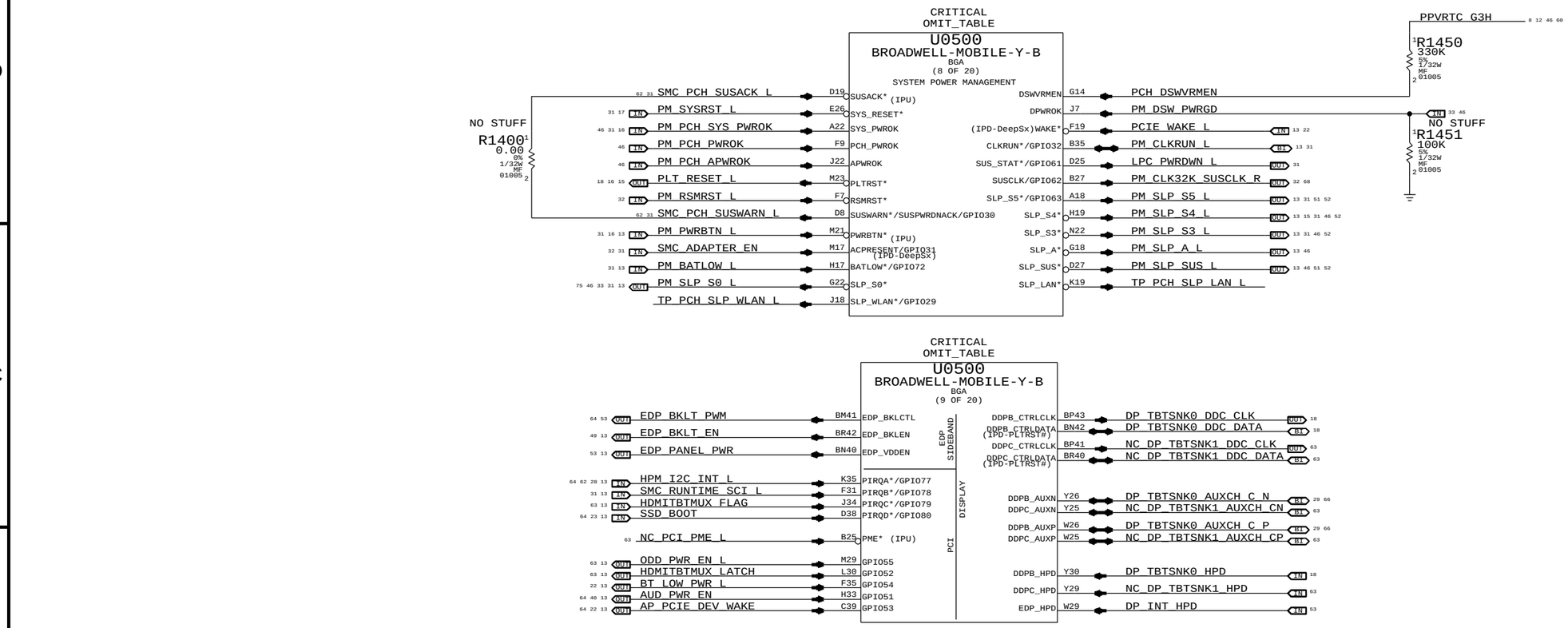

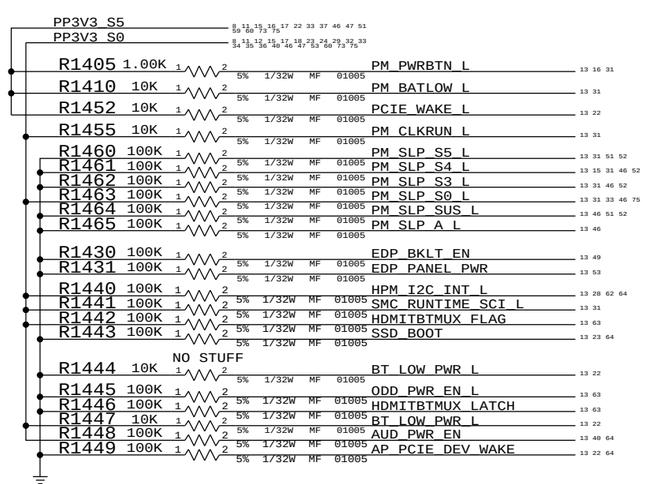

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PAGE TITLE
PCH PM/PCI/GFX

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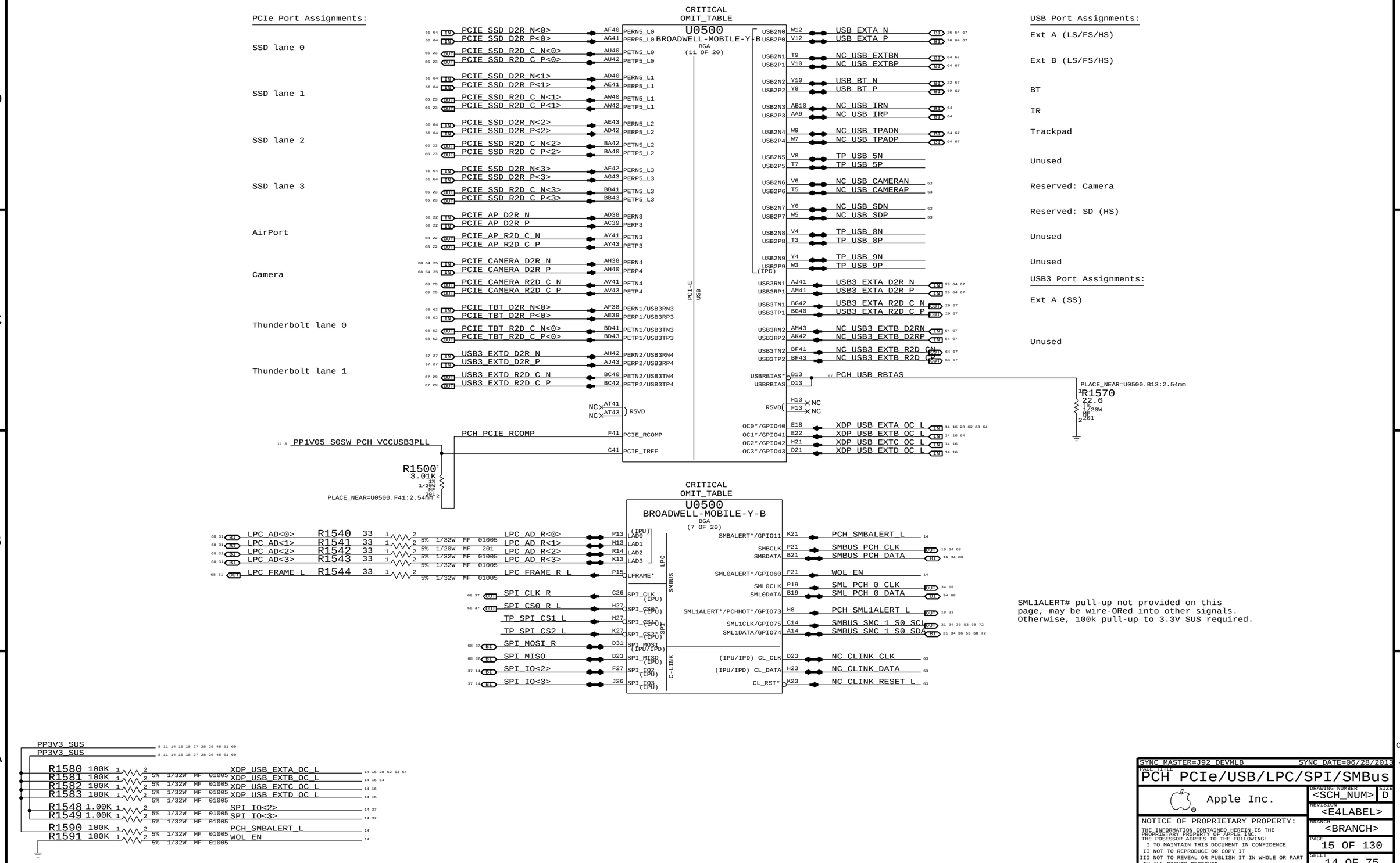

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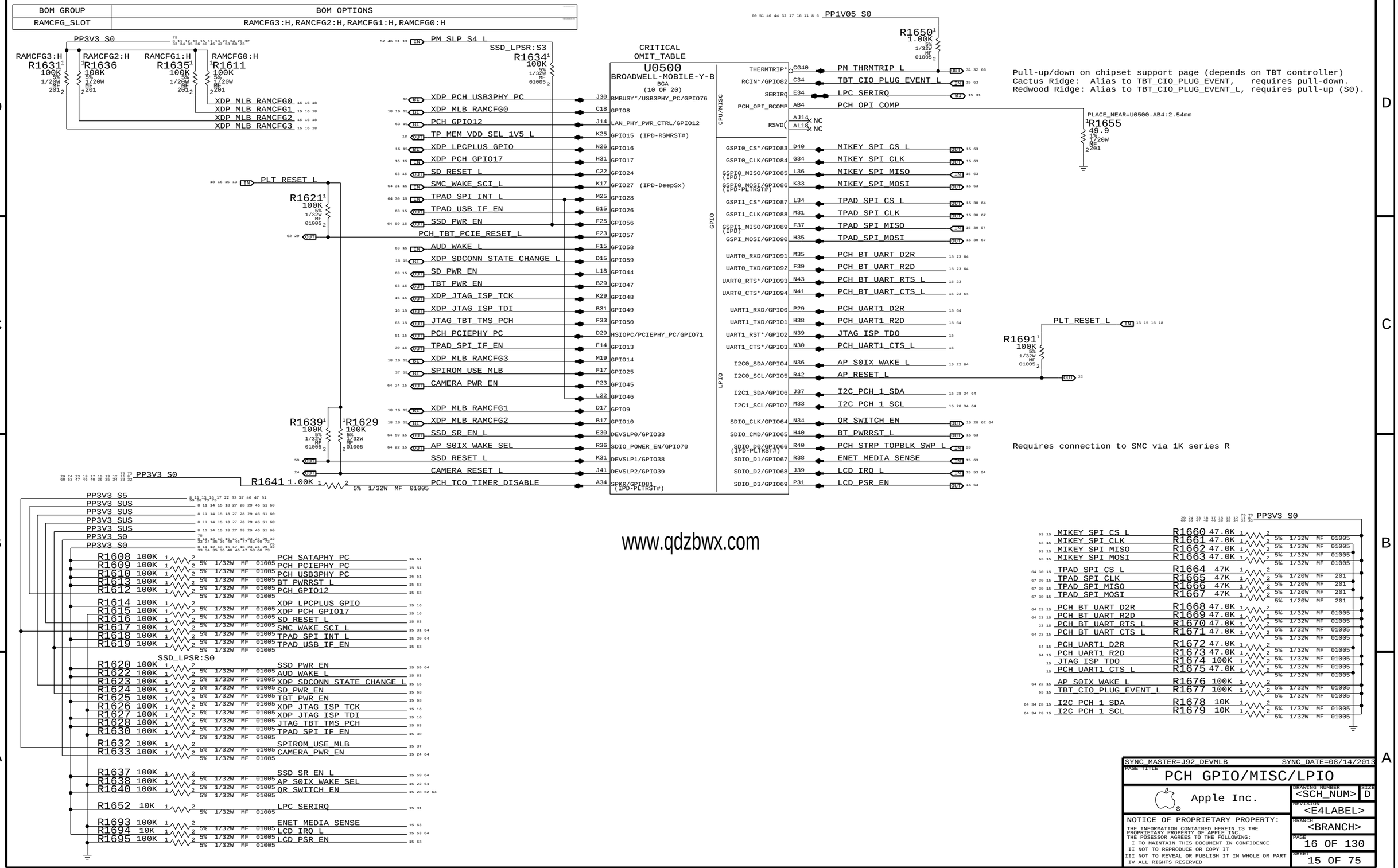
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H



Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

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PAGE TITLE
PCH GPIO/MISC/LPIO

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Merged (CPU/PCH) Micro2-XDP

Extra BPM Probepoints

XDP_BPM_L<2> — PP1802
XDP_BPM_L<3> — PP1803
XDP_BPM_L<4> — PP1804
XDP_BPM_L<5> — PP1805
XDP_BPM_L<6> — PP1806
XDP_BPM_L<7> — PP1807

CPU_VCCST_PWRGD — R1800 1K XDP — PLACE_NEAR=U0500.BU14:2.54mm
PM_PWRBTN_L — R1802 0 XDP — PLACE_NEAR=U5000.K1:2.54mm
PM_PCH_SYS_PWROK — R1804 0 XDP
XDP_CPU_TCK
PCH_JTAGX — R1835 0 XDP — PLACE_NEAR=J1800.58:28mm

PP1V05_S0

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

R1830 150 5% 1/20W MF 201

XDP_CPU_PREQ_L	OBSFN_A0	OBSFN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSFN_A1	OBSFN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSFN_B0	OBSFN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSFN_B1	OBSFN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG_L	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

518S0847

C1804 0.1UF 10% 6.3V CERM-X5R 0201
R1831 1K 5% 1/20W MF 201
C1800 0.1UF 10% 6.3V CERM-X5R 0201
C1801 0.1UF 10% 6.3V CERM-X5R 0201
C1806 0.1UF 10% 6.3V CERM-X5R 0201

XDP_CPU_PRESENT_L
NOSTUFF
R1832 0 5% 1/20W MF 0201

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

R1805 1K XDP — PLT_RESET_L — PLACE_NEAR=U0500.AG7:2.54mm

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS

CRITICAL
Q1840 XDP DMN5L06VK-7 SOT563 — XDP_CPU_TDO — PLACE_NEAR=J1800.55:28mm
CRITICAL
Q1840 XDP DMN5L06VK-7 SOT563 — XDP_CPUPCH_TRST_L — PLACE_NEAR=J1800.55:28mm — MAKE_BASE=TRUE
CRITICAL
Q1842 XDP DMN5L06VK-7 SOT563 — XDP_CPU_TDI — PLACE_NEAR=J1800.55:28mm
CRITICAL
Q1842 XDP DMN5L06VK-7 SOT563 — XDP_CPU_TMS — PLACE_NEAR=J1800.55:28mm

R1810 51 XDP — XDP_CPU_TDO — PLACE_NEAR=U0500.CU38:28mm
R1813 51 XDP — XDP_CPU_TCK — PLACE_NEAR=U0500.CM41:28mm

TDI and TMS are terminated in CPU.

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals		Non-XDP Signals
XDP_MLB_RAMCFG0		
XDP_USB_EXTA_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L	MAKE_BASE=TRUE	XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	PP1873	
XDP_USB_EXTD_OC_L	PP1874	
XDP_SDCONN_STATE_CHANGE_L	PP1875	
XDP_MLB_RAMCFG1		
XDP_MLB_RAMCFG2		
XDP_MLB_RAMCFG3		
XDP_JTAG_ISP_TCK	PP1879	
XDP_FW_PME_L	PP1880	
XDP_PCH_SATAPHY_PC	R1881 SHORT OMIT NONE NONE NONE 201	PCH_SATAPHY_PC
XDP_PCH_UART_SSD_L_BT_H	R1882 SHORT OMIT NONE NONE NONE 201	PCH_UART_SSD_L_BT_H
XDP_SSD_PCIE0_SEL_L	R1883 1K 5% 1/20W MF 201	
XDP_LPCPLUS_GPIO	PP1884	
XDP_PCH_GPIO17	PP1885	
XDP_PCH_USB3PHY_PC	R1886 SHORT OMIT NONE NONE NONE 201	PCH_USB3PHY_PC
XDP_JTAG_ISP_TDI	PP1887	

Unused & MLB_RAMCFGx GPIOs have TPs.
USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.
SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.
JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.
NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.
SSD_PCIEx_SEL_L straps are connected via 1K to common net.
LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
C1845 0.1UF 10% 10V X5R-CERM 0201
U1845 VCC 74LVC1G07GF SOT891 GND
R1845 330K 5% 1/20W MF 201
ALL_SYS_PWRGD
XDP_JTAG_CPU_ISOL_L

PP1V05_SUS

PCH_JTAGX	R1899 1K	NO STUFF
XDP_PCH_TDO	R1890 51	XDP
XDP_PCH_TDI	R1891 51	XDP
XDP_PCH_TMS	R1892 51	XDP
XDP_PCH_TCK	R1896 51	NO STUFF
XDP_CPUPCH_TRST	R1897 51	NO STUFF

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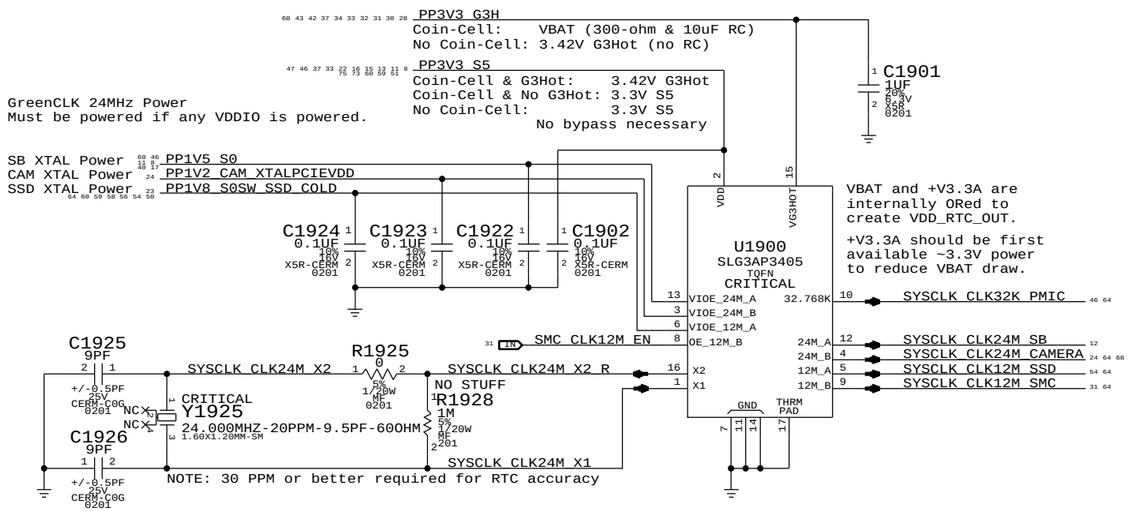
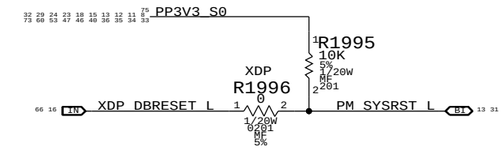
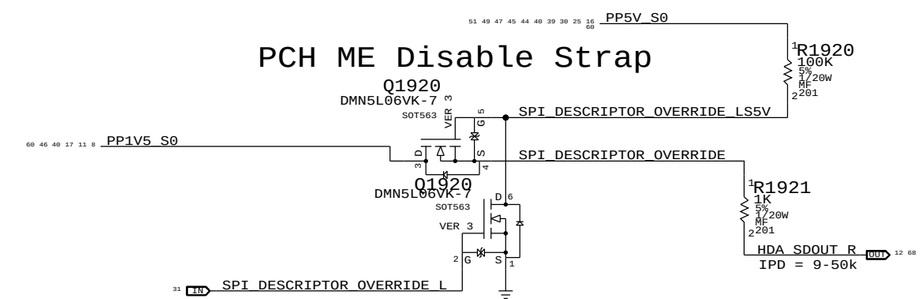
System 32kHz / 12MHz / 24MHz Clock Generator

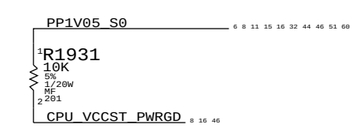




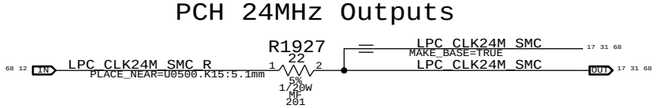
PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



PCH 24MHz Outputs



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Chipset Support

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Platform Reset Connections

Unbuffered

16 15 13 IN PLT_RESET_L — R2072 0 5% 1/20W MF 0201 — SMC_LRESET_L OUT 31

29 24 23 18 17 15 13 12 11 23 60 53 47 46 40 36 35 34 33 32 PP3V3_S0

R2001 2.2K 5% 1/20W MF 201

13 DP_TBTSNK0_DDC_DATA

13 DP_TBTSNK0_DDC_CLK

R2000 2.2K 5% 1/20W MF 201

PP3V3_SUS 8 11 14 15 27 28 29 46 51 60

R2010 100K 5% 1/20W MF 201

33 14 OUT PCH_SML1ALERT_L

PP3V3_S0 75 8 11 12 13 15 17 18 23 24 29 32 33 34 35 36 40 46 47 53 60 73

CRITICAL

74LVC1G08 SOT891

13 OUT DP_TBTSNK0_HPD

U2020 08

E85_TEST_MODE_HPD IN 29

DP_E85SNK_HPD IN 28 33 64

C2020 0.1UF 10V X5R-CERM 0201

NC

R2020 4.7K 5% 1/20W MF 201

RAM Configuration Straps

Pull-downs for chip-down RAM systems

16 15 OUT XDP_MLB_RAMCFG0

16 15 OUT XDP_MLB_RAMCFG1

16 15 OUT XDP_MLB_RAMCFG2

16 15 OUT XDP_MLB_RAMCFG3

RAMCFG3:L	RAMCFG2:L	RAMCFG1:L	RAMCFG0:L
R2050 10K 5% 1/20W MF 201	R2051 10K 5% 1/20W MF 201	R2052 10K 5% 1/20W MF 201	R2053 10K 5% 1/20W MF 201

LPDDR3 Alias Support

18 6 IN TP_CPU_MEM_RESET_L — TP_CPU_MEM_RESET_L 6 18

MAKE_BASE=TRUE

18 15 IN TP_MEM_VDD_SEL_1V5_L — TP_MEM_VDD_SEL_1V5_L 15 18

MAKE_BASE=TRUE

69 20 19 18 PPVREF_S3_MEM_VREFDQ_A — PPVREF_S3_MEM_VREFDQ_A 18 19 20 69

MAKE_BASE=TRUE VOLTAGE=0.6V

69 21 19 18 PPVREF_S3_MEM_VREFDQ_B — PPVREF_S3_MEM_VREFDQ_B 18 19 21 69

MAKE_BASE=TRUE VOLTAGE=0.6V

69 21 20 19 18 PPVREF_S3_MEM_VREFCA — PPVREF_S3_MEM_VREFCA 18 19 20 21 69

MAKE_BASE=TRUE VOLTAGE=0.6V

PPVREF_S3_MEM_VREFCA 18 19 20 21 69

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Project Chipset Support

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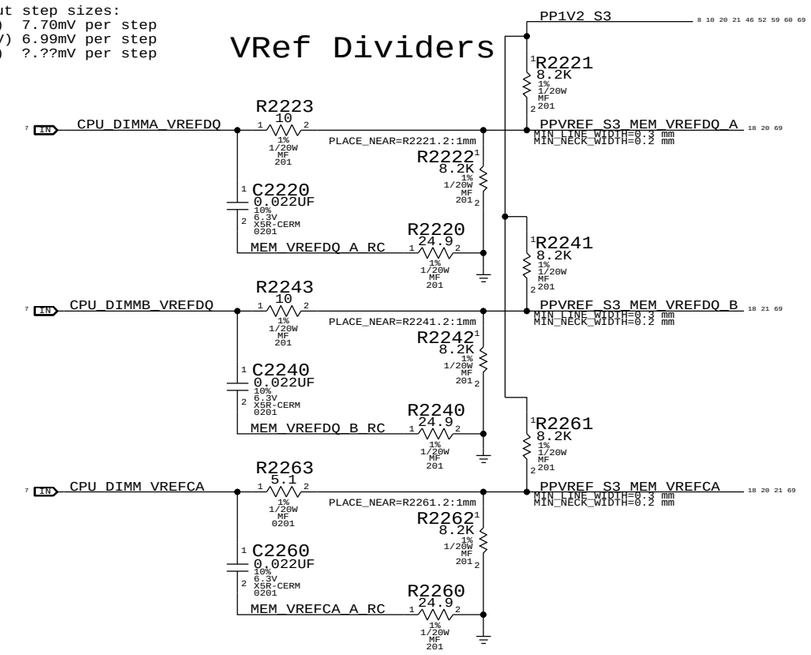
CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

VRef Dividers



SYNC MASTER=J92 DEVMLB SYNC DATE=06/28/2013

PAGE TITLE
LPDDR3 VREF MARGINING

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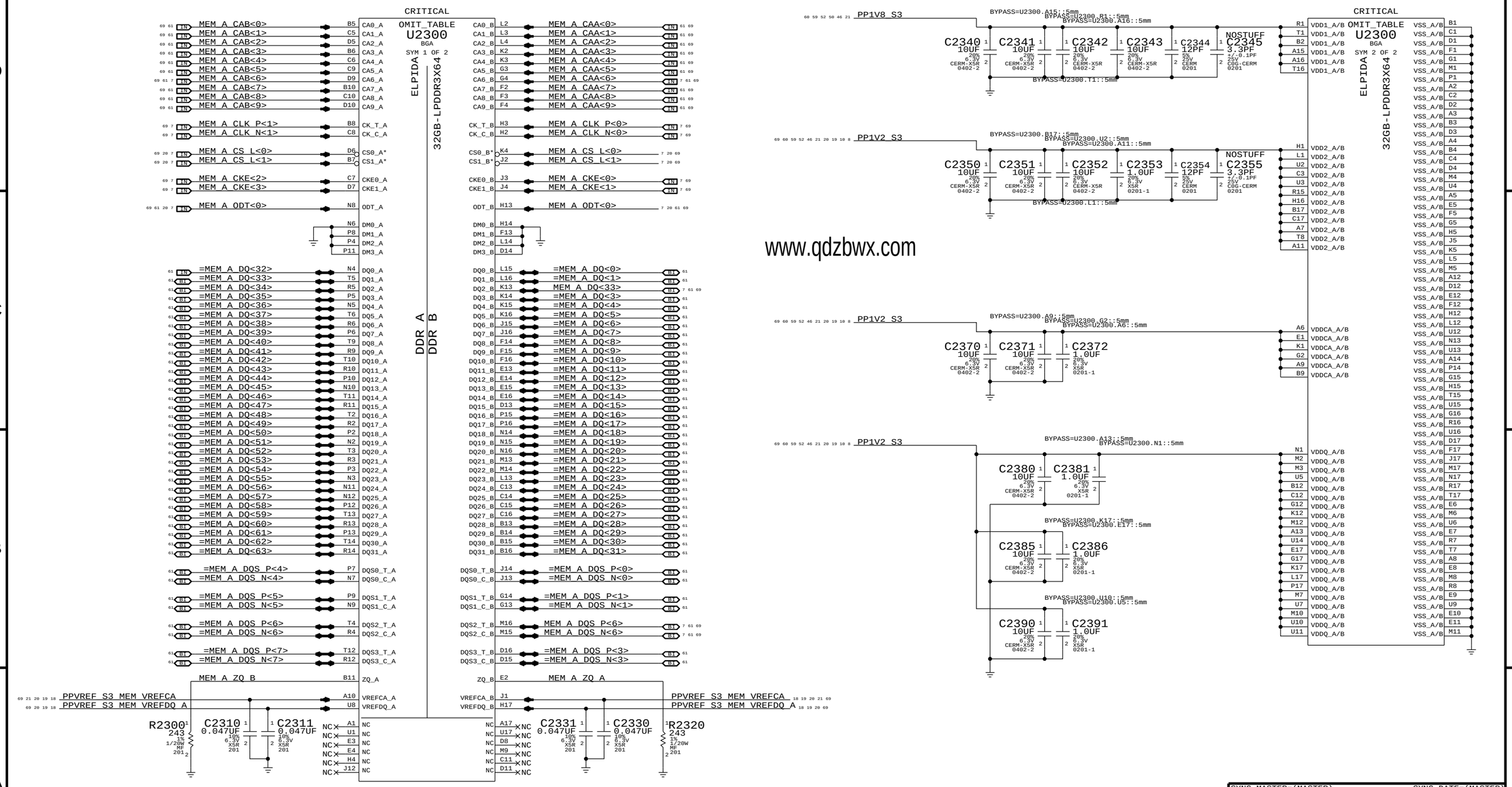

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PAGE TITLE

LPDDR3 DRAM Channel A (0-63)

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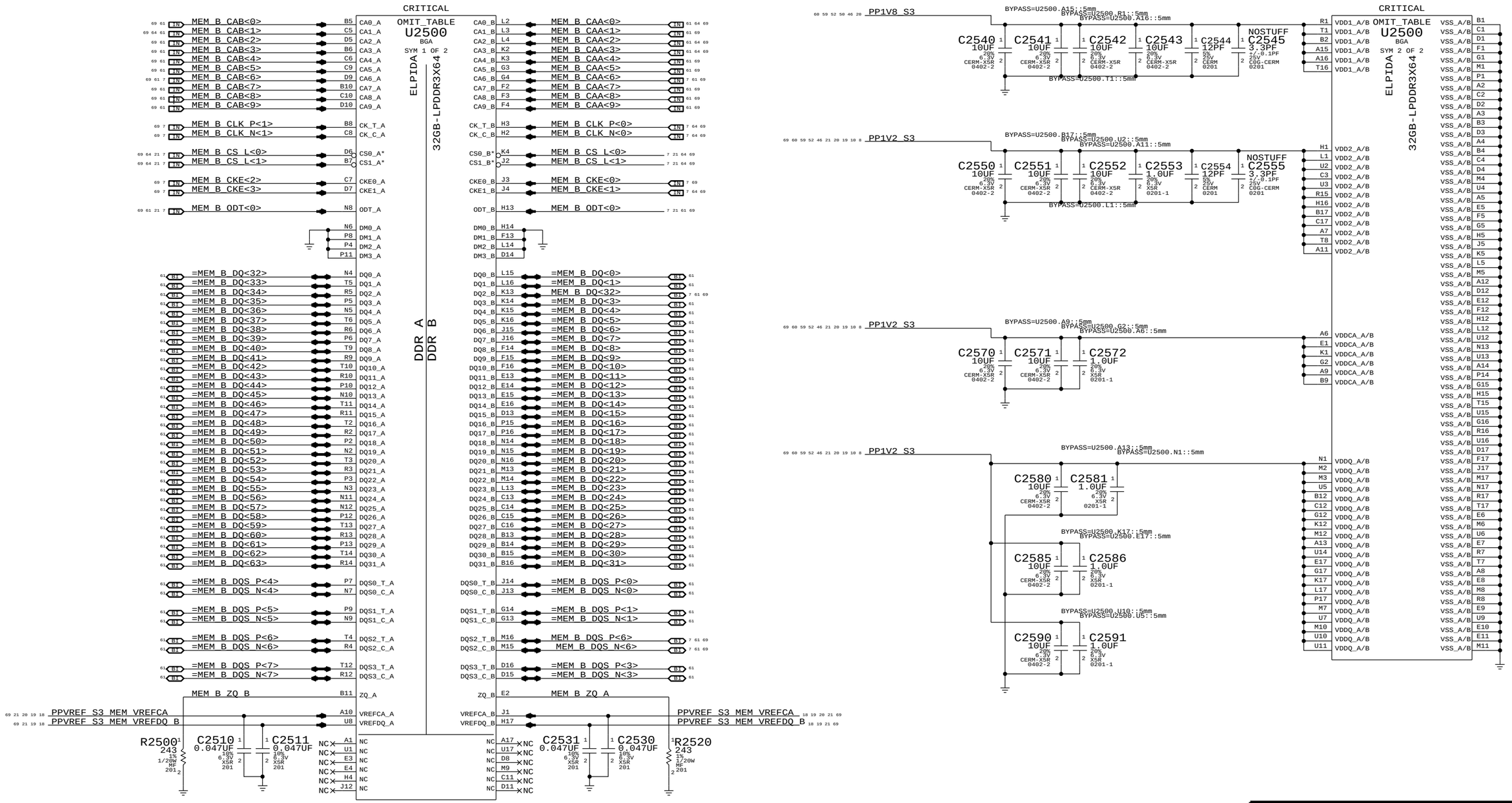

SYNC MASTER=(MASTER) SYNC DATE=(MASTER)

PAGE TITLE

LPDDR3 DRAM Channel B (0-63)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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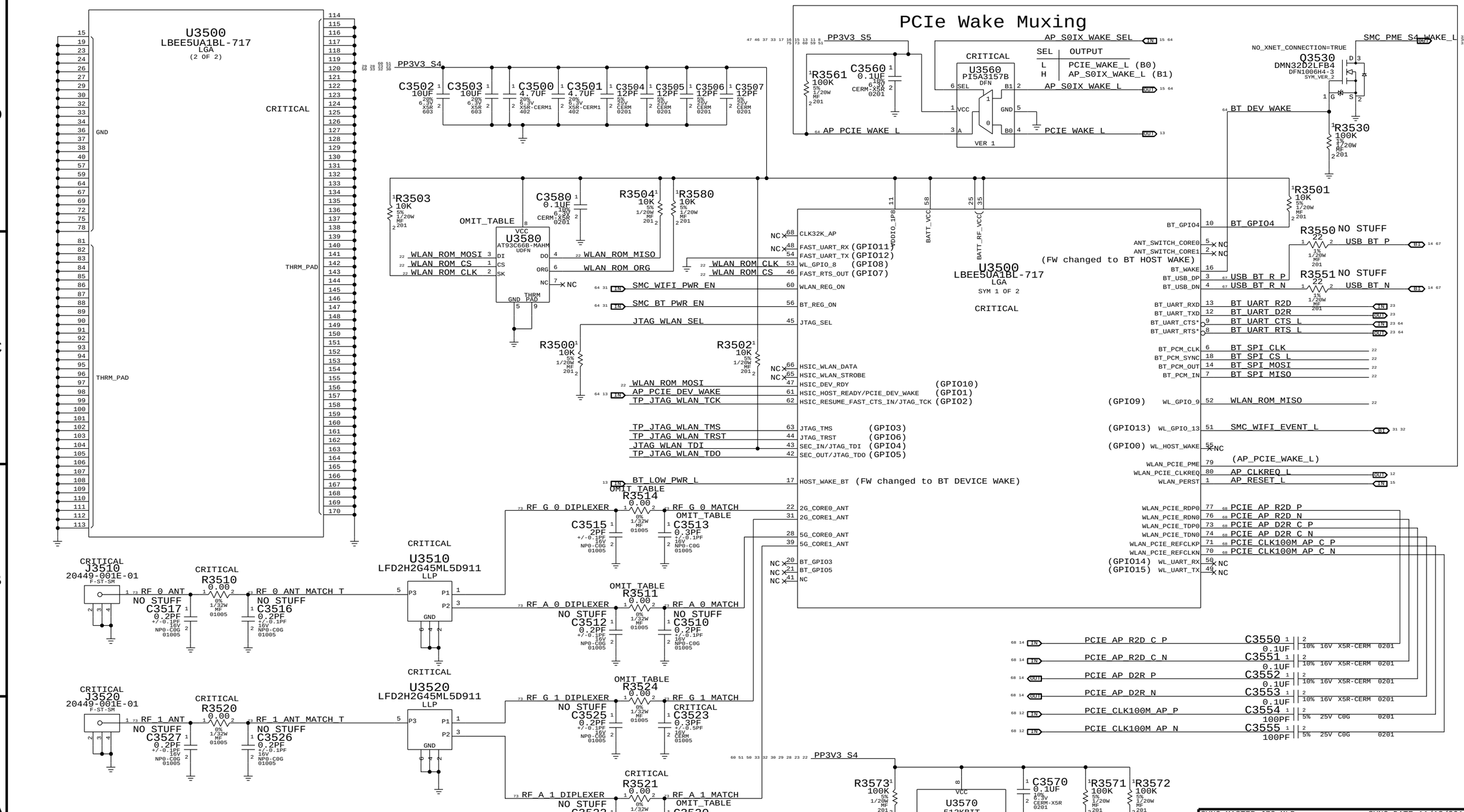

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S0259	1	CAP,7PF,+/-0.1PF,16V,01005	R3514	CRITICAL	
152S1742	1	IND,FILM,1.6NH,+/-0.1NH,200MA,01005	C3513	CRITICAL	
152S1544	1	IND,FILM,0.4NH,+/-0.1NH,270MA,01005	R3511	CRITICAL	
152S1564	1	IND,FILM,2.4NH,+/-0.1NH,200MA,01005	R3524	CRITICAL	
152S1720	1	IND,FILM,1.8NH,+/-0.1NH,270MA,01005	C3520	CRITICAL	

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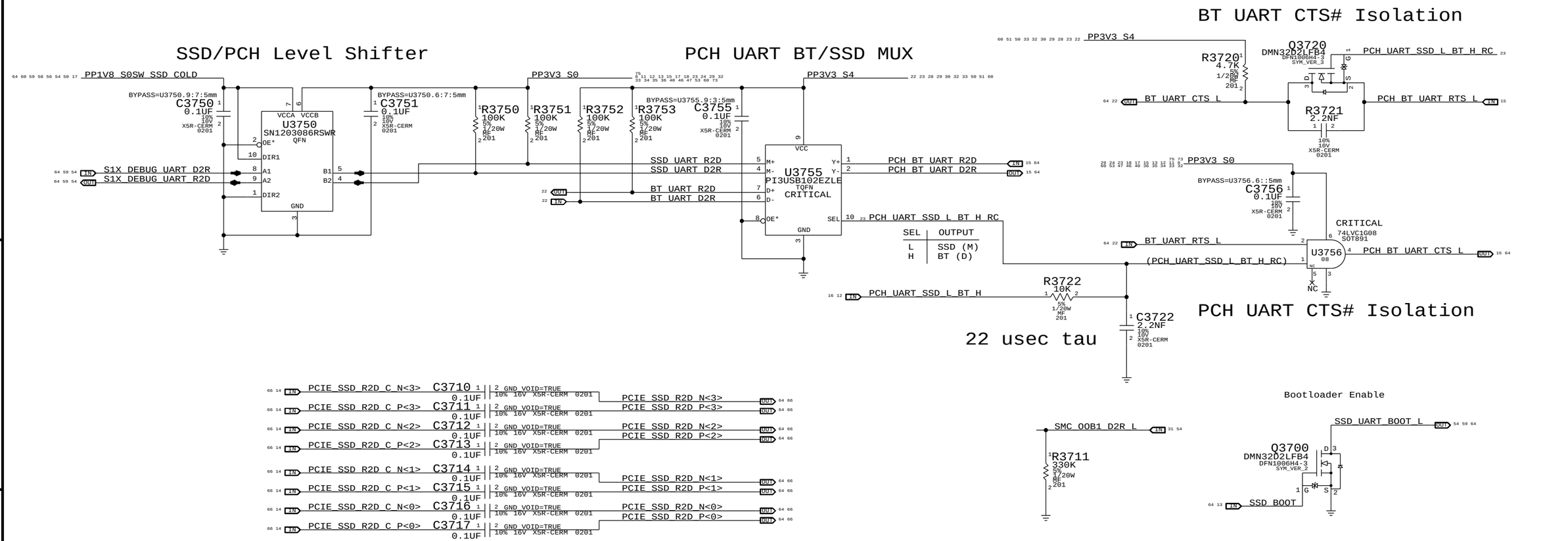

SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/11/2013

PAGE TITLE
SSD Support

Apple Inc.

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BRANCH <BRANCH>

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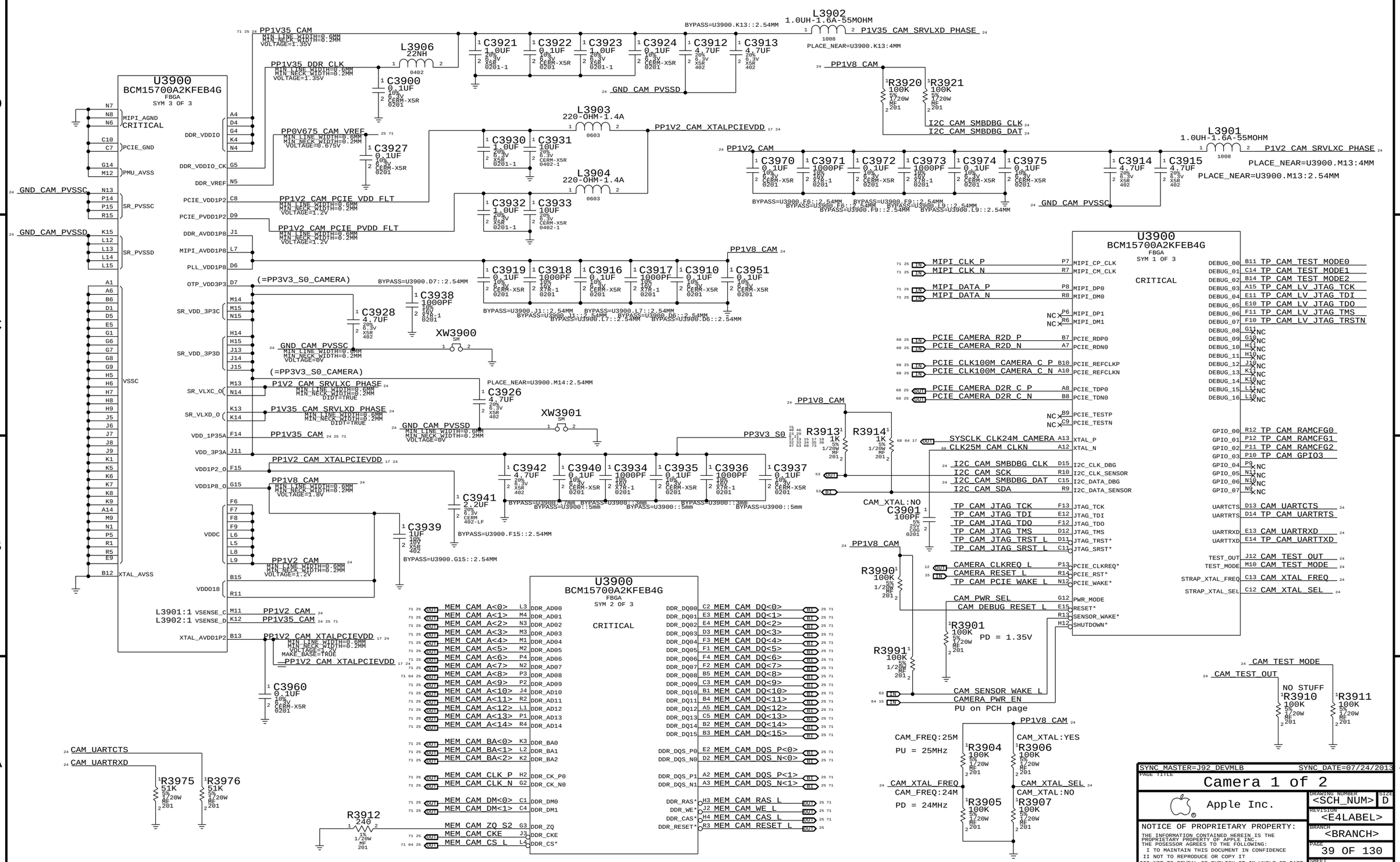

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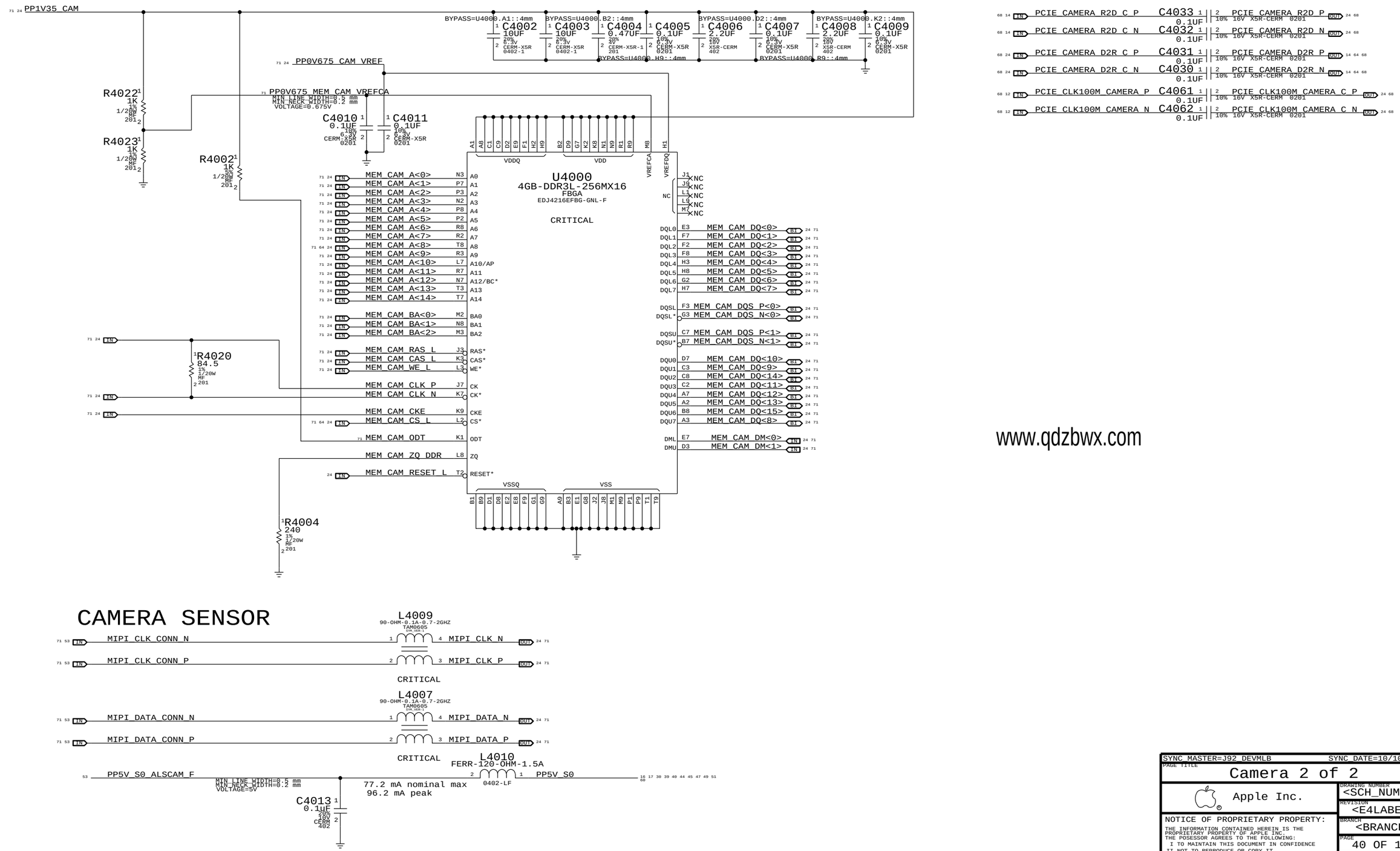

www.qdzbwx.com

SYNC_MASTER=J92_DEVMLB	SYNC_DATE=10/10/2013
PAGE TITLE: Camera 2 of 2	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
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	PAGE: 40 OF 130
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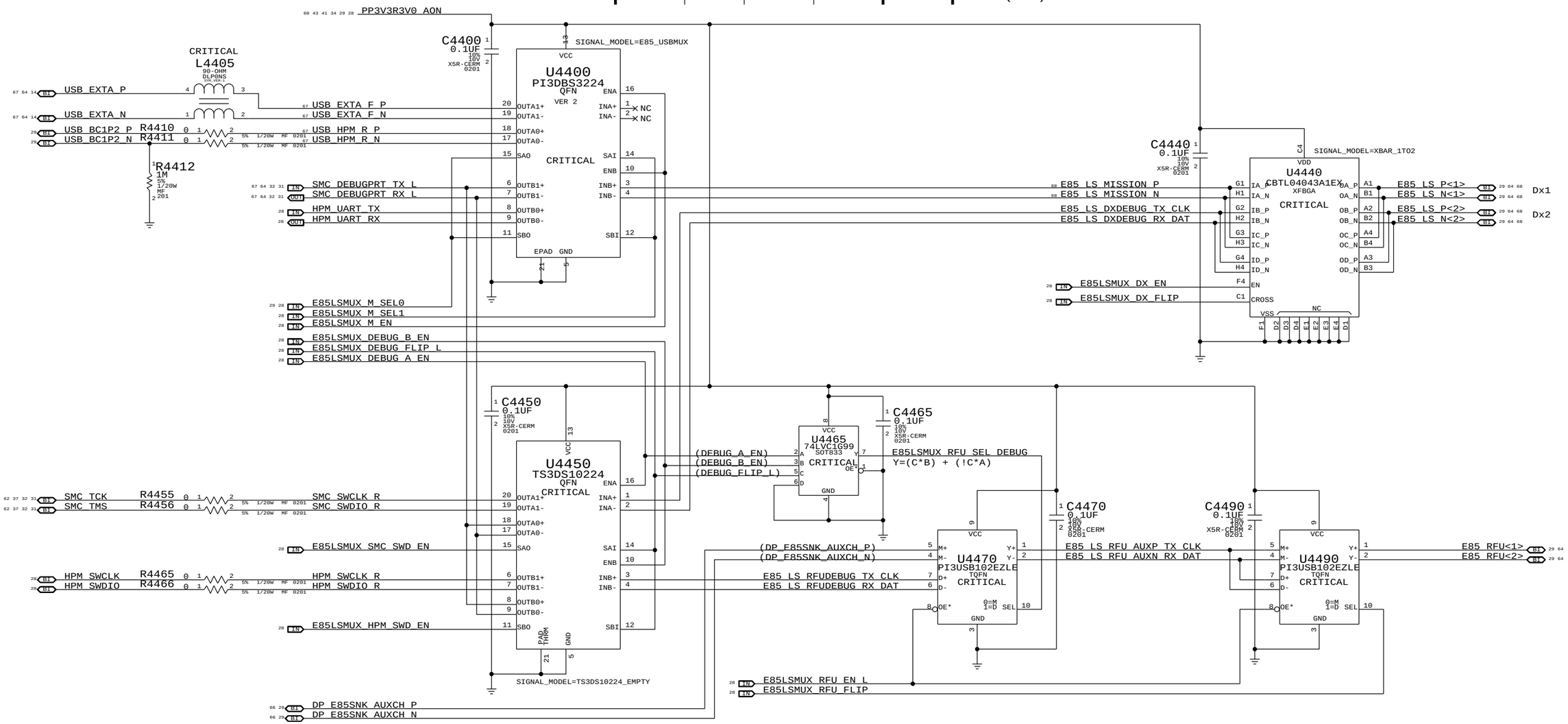
Mode	DX_EN	M_EN	M_SEL0	M_SEL1	INB	Mission
Empty	0	0	X	X	Hi-Z	Hi-Z
Mojo	1	1	1	1	OUTB1	UART (SMC)
USB (Host)	1	1	1	0	OUTA1	USB (PCH)
USB (Device)	1	1	0	0	OUTA0	USB (HPM)
HPM UART	1	1	0	1	OUTB0	UART (HPM)



Mode	DX_EN	DEBUG_A_EN	DEBUG_B_EN	DEBUG_FLIP_L	SMC_SWD_EN	HPM_SWD_EN	INA	DXDEBUG
Empty	0	0 X	X 0	1 0	X	X	Hi-Z	Hi-Z
No Debug	1	0 X	X 0	1 0	X	X	Hi-Z	Hi-Z
SMC SWD	1	1	X	1	1	X	OUTA1	SWD (SMC)
Mojo	1	1 X	X 1	1 0	0 X	X 0	OUTA0 OUTB0	UART (SMC)
HPM SWD	1	X	1	0	X	1	OUTB1	SWD (HPM)

Mode	RFU_EN_L	DEBUG_A_EN	DEBUG_B_EN	DEBUG_FLIP_L	SMC_SWD_EN	HPM_SWD_EN	INB	RFU
Empty	1	X 0	0 X	1 0	X	X	Hi-Z	Hi-Z
DP	0	X 0	0 X	1 0	X	X	Hi-Z	AUX+/HPD
HPM SWD	0	X	1	1	X	1	OUTB1	SWD (HPM)
Mojo	0	X 1	1 X	1 0	X 0	0 X	OUTB0 OUTA0	UART (SMC)
SMC SWD	0	1	X	0	1	X	OUTA1	SWD (SMC)

SYNC_MASTER=J92_DEVMLB SYNC_DATE=07/08/2014

PAGE TITLE
Low Speed MUXing

Apple Inc.

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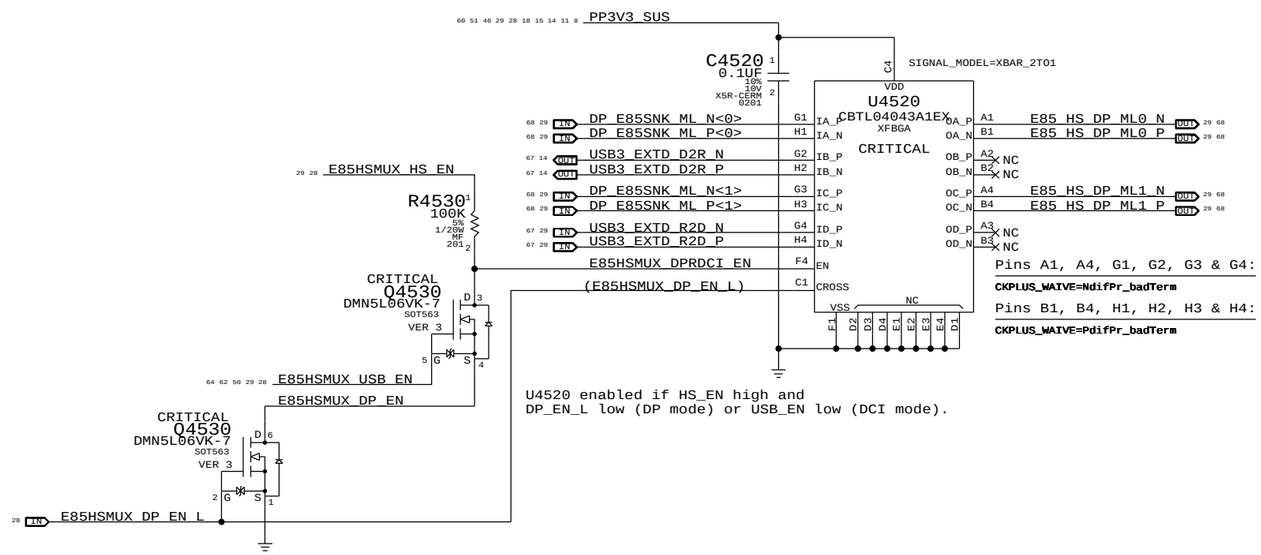

HS_FLIP swaps Tx1/2 and Rx1/2

Mode	HS_EN	DP_EN_L	USB_EN	SSTx1	SSRx1	SSTx2	SSRx2
Empty	0	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
USB3	1	1	1	R2D	D2R	Hi-Z	Hi-Z
USB3/DPx2	1	0	1	R2D	D2R	ML1	ML0
DPx4 (Passive)	1	0	0	ML2	ML3	ML1	ML0
DCI (Debug)	1	1	0	(ML2)	(ML3)	DCI-R2D	DCI-D2R

NOTE: Invert HS_FLIP in DCI mode to put DCI-USB on USB3 pins. USB3 and DP not usable in DCI mode.

SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014

PAGE TITLE
High Speed MUXing

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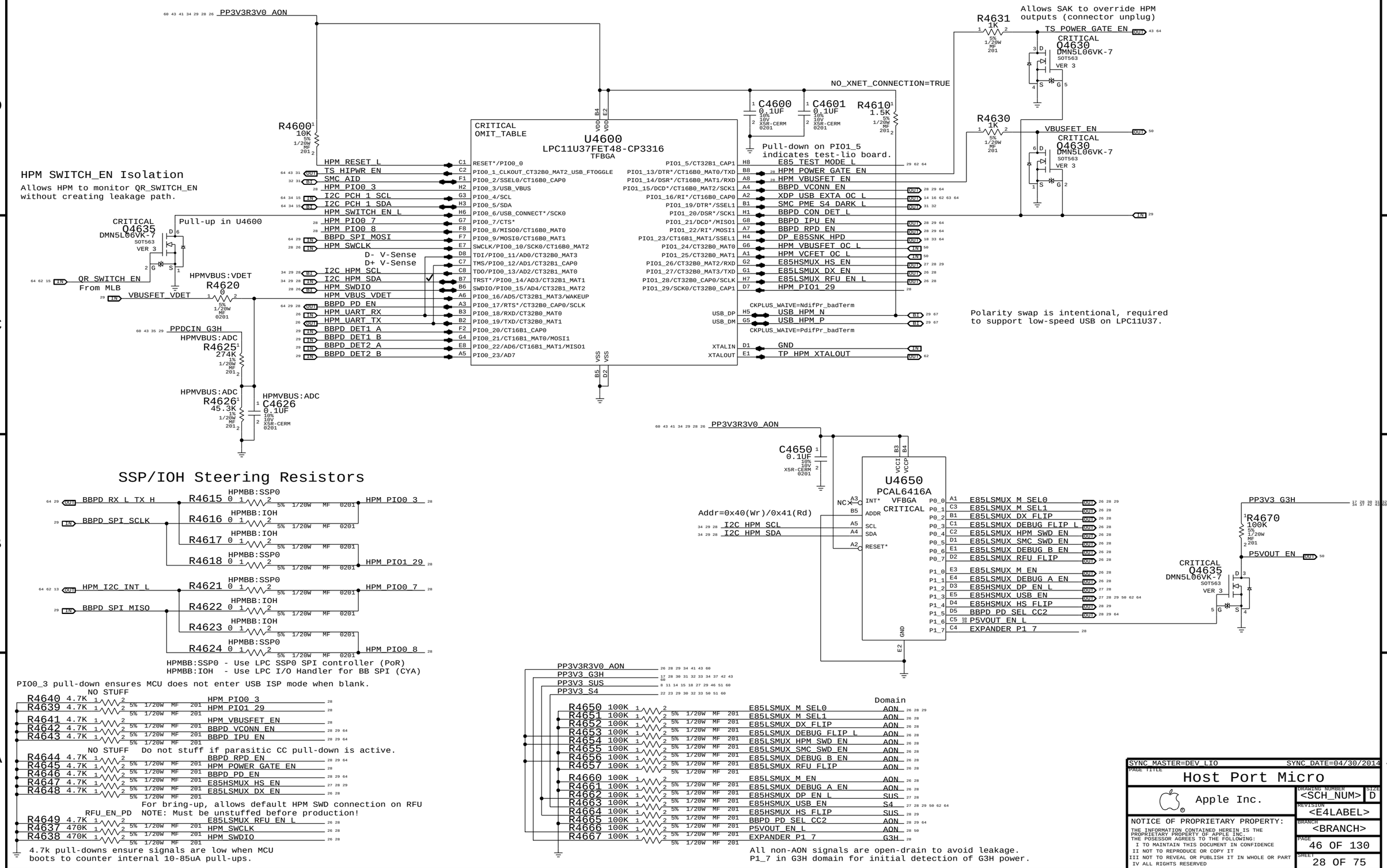

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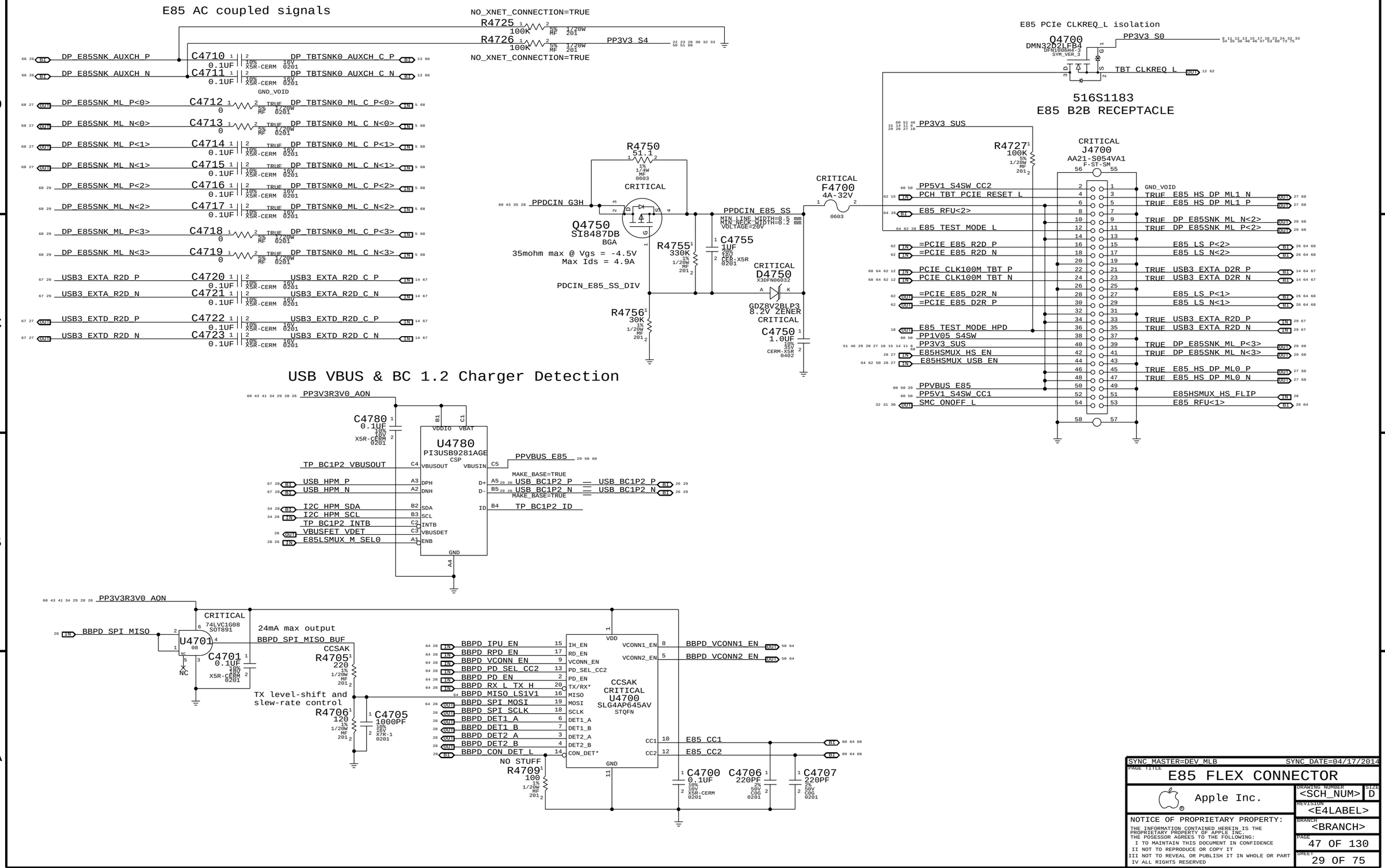

SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014

PAGE TITLE: E85 FLEX CONNECTOR

Apple Inc.

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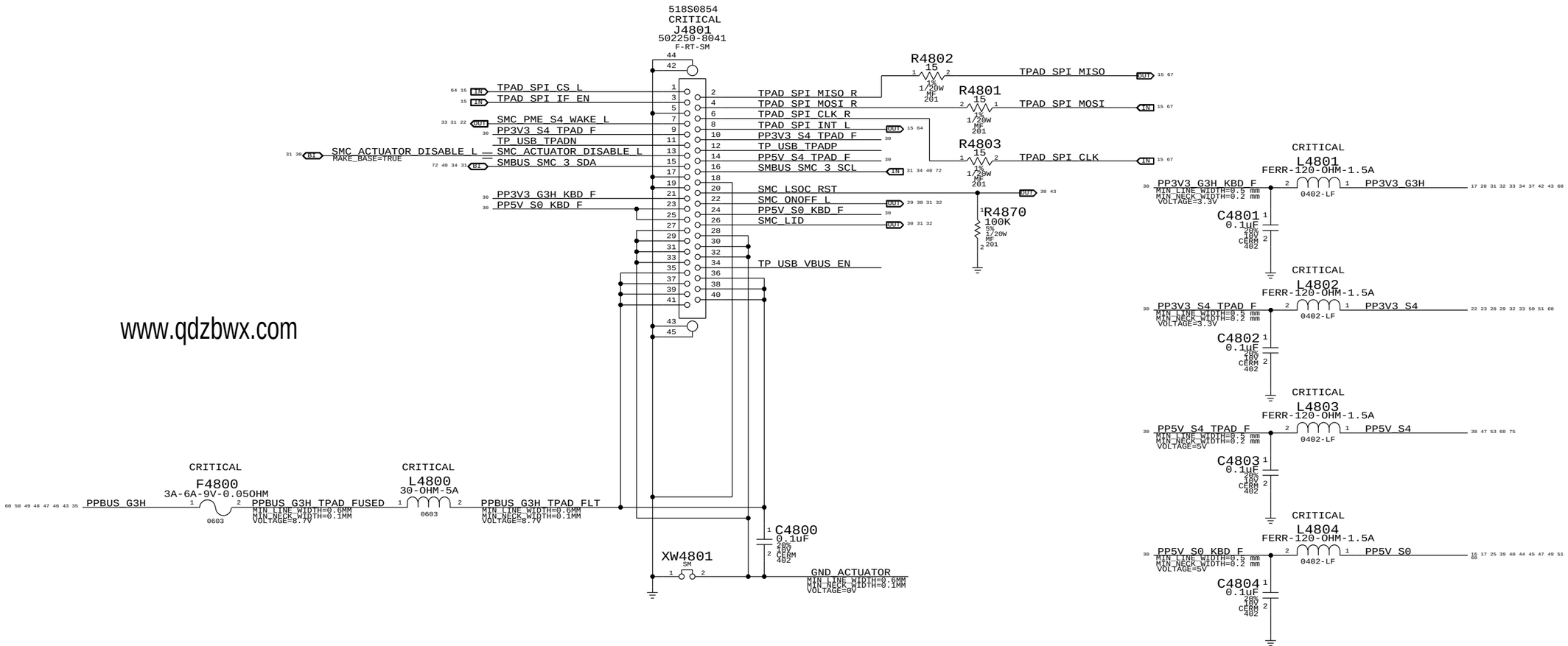
IPD ZIF CONNECTOR

Bottom side contacts used
Pinout reversed from flex



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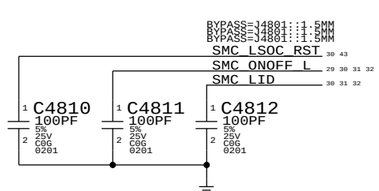

SYNC_MASTER=J92_DEVMLB SYNC_DATE=03/26/2014

PAGE TITLE
Keyboard & Trackpad Conn

Apple Inc.

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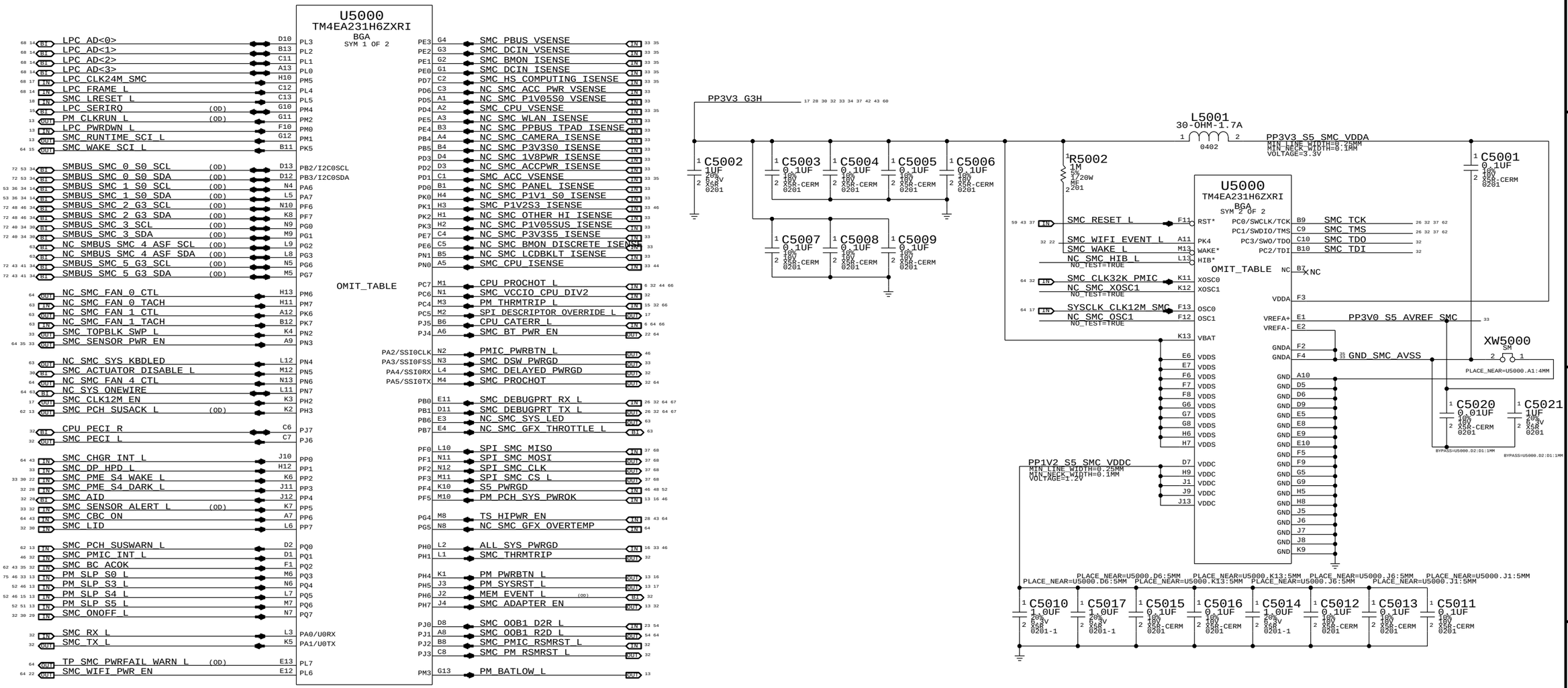

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC_MASTER=J92_DEVMLB SYNC_DATE=10/11/2013

PAGE TITLE
SMC

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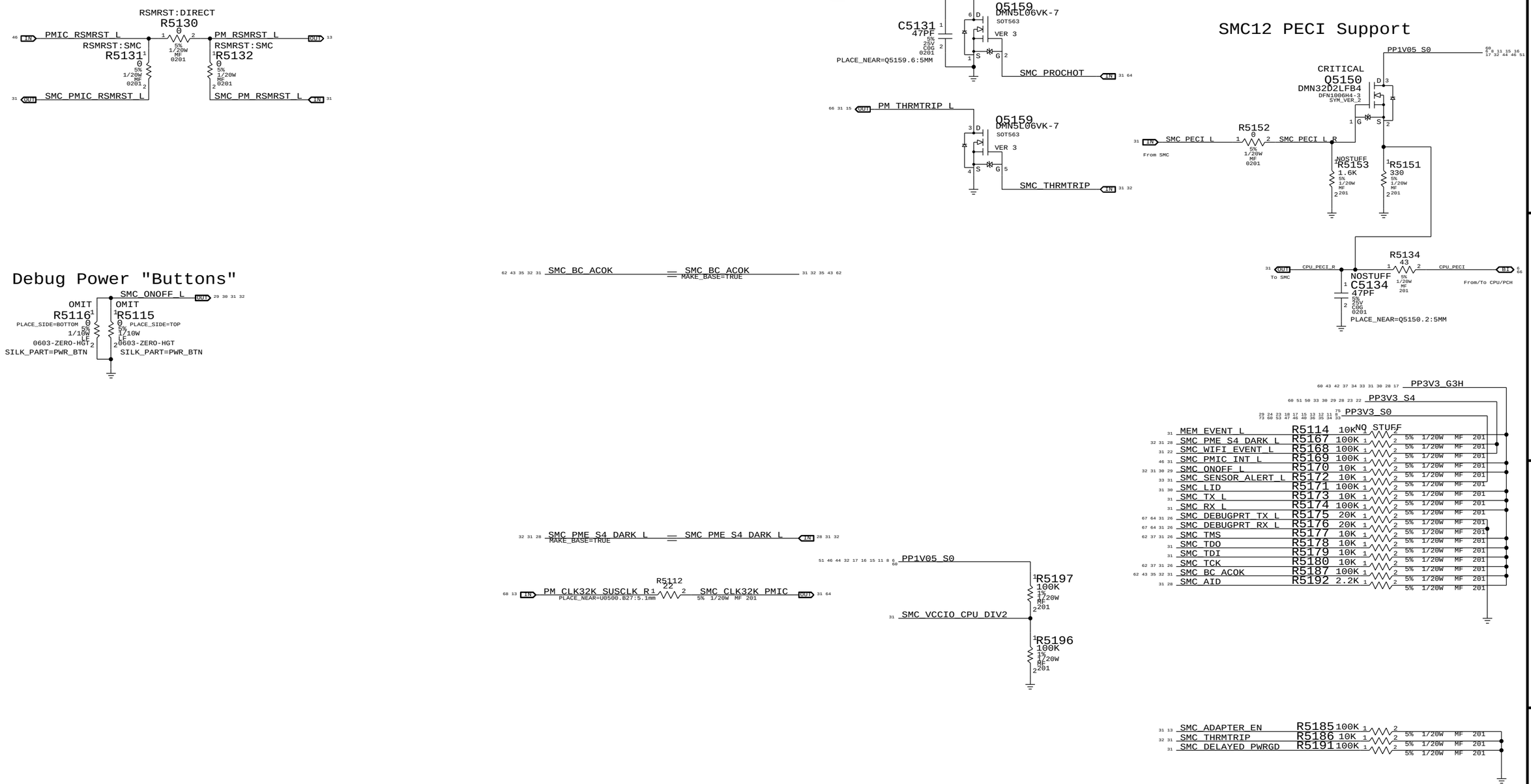

SYNC_MASTER=J92_DEVMLB SYNC_DATE=10/11/2013

PAGE TITLE
SMC Shared Support

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DRAWING NUMBER <SCH_NUM> SIZE D

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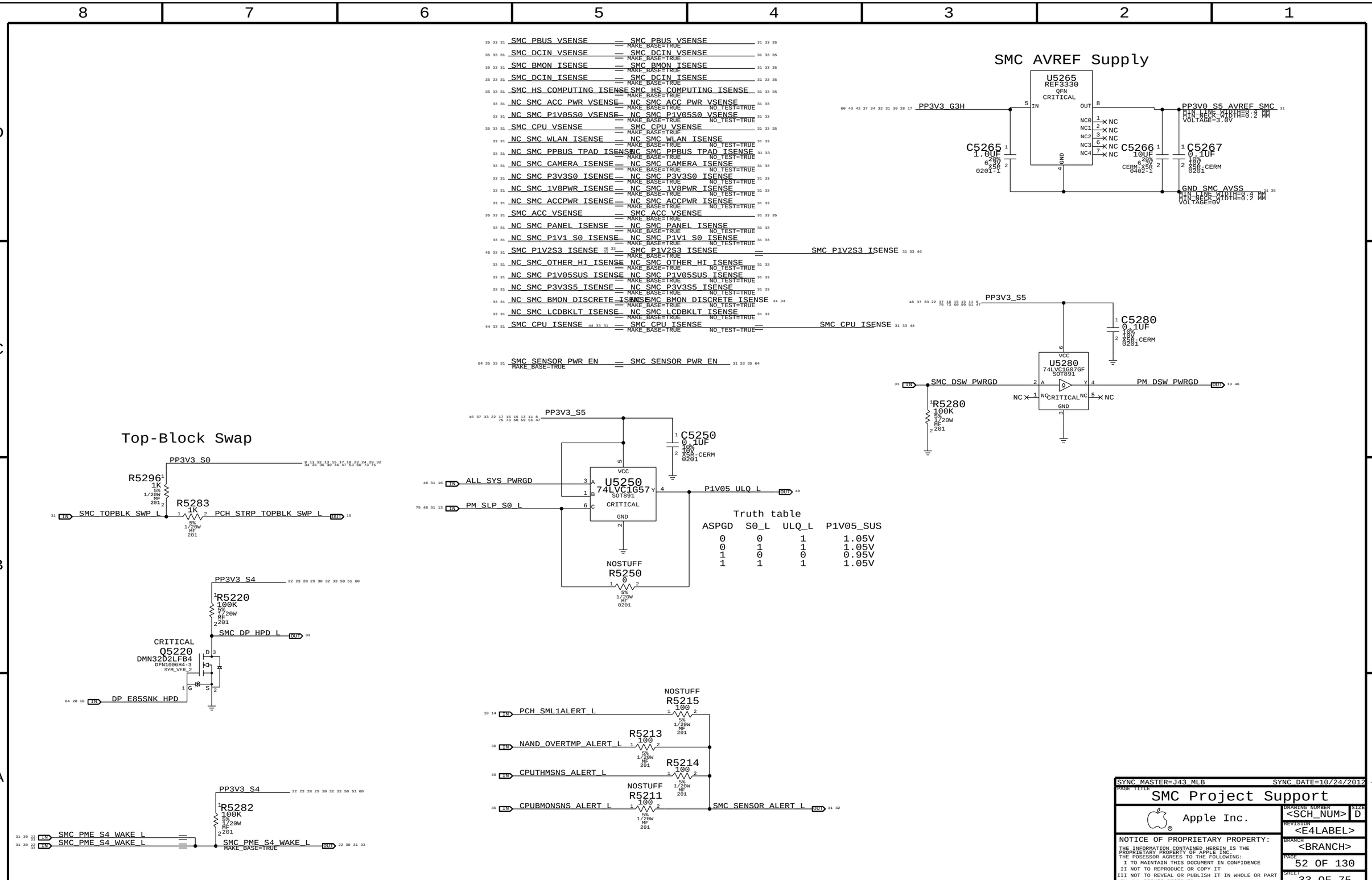

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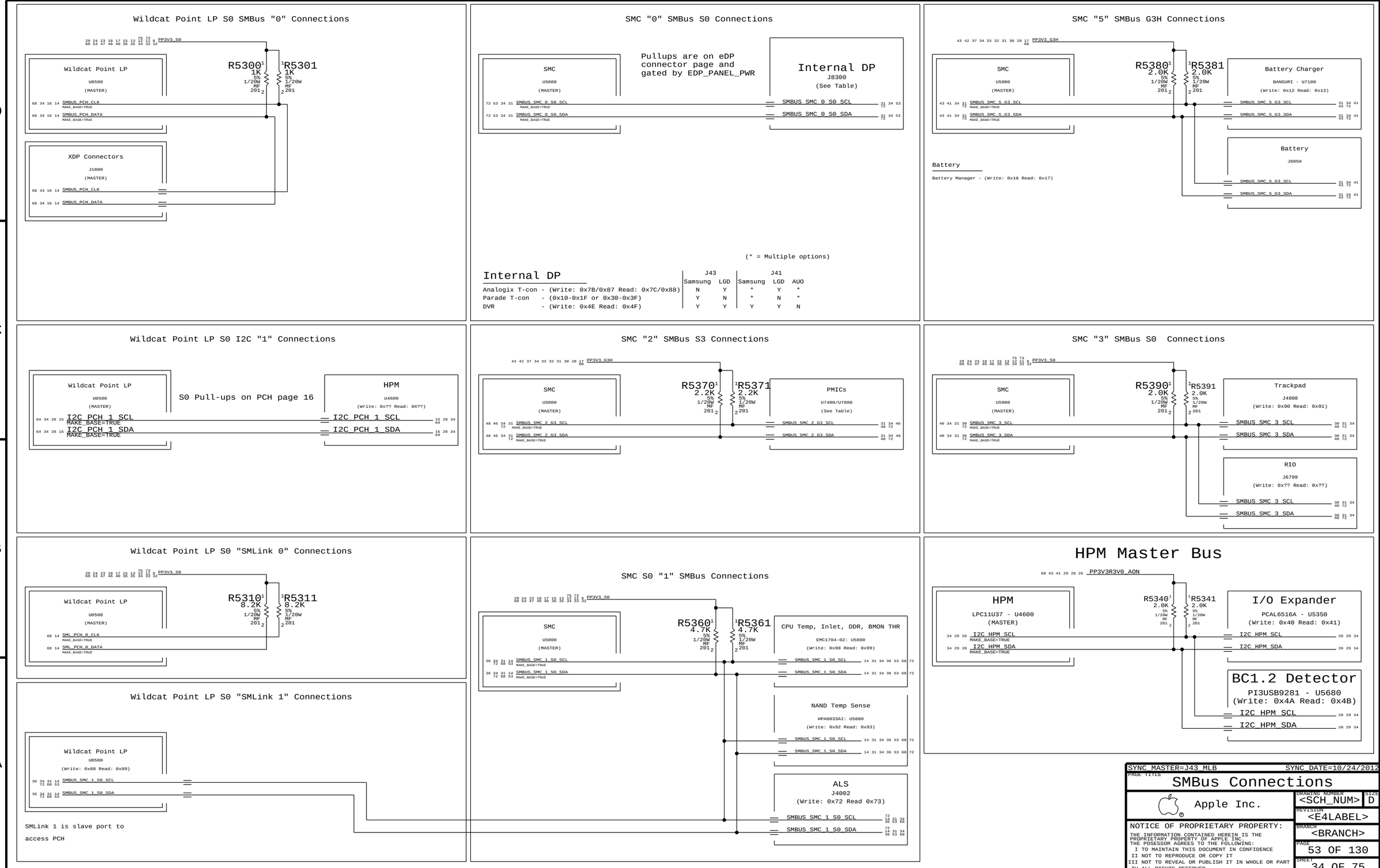

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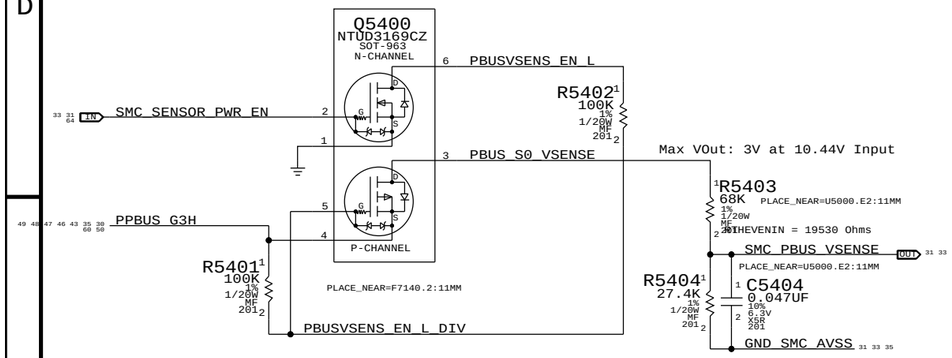
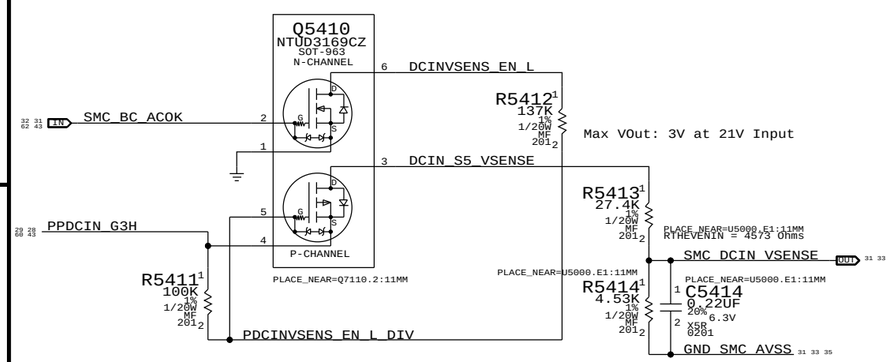
POR VOLTAGE / CURRENT SENSORS : TO BE USED IN PRODUCTION

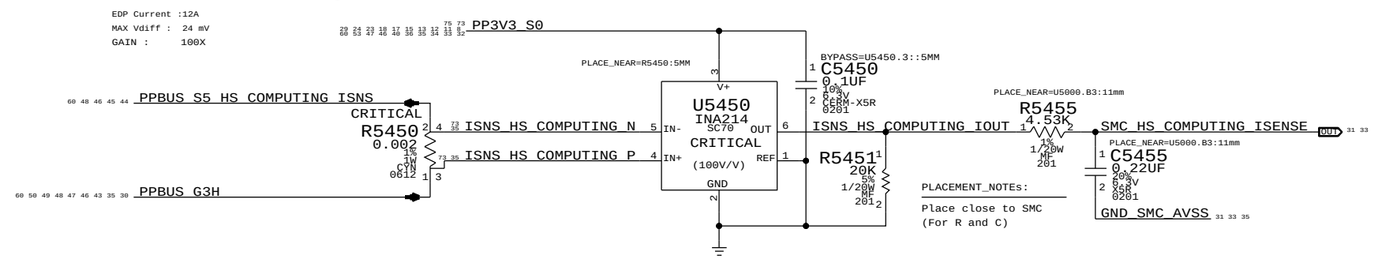
VP0R: PBUS Voltage Sense Enable & Filter



VD0R: DC-In Voltage Sense Enable & Filter

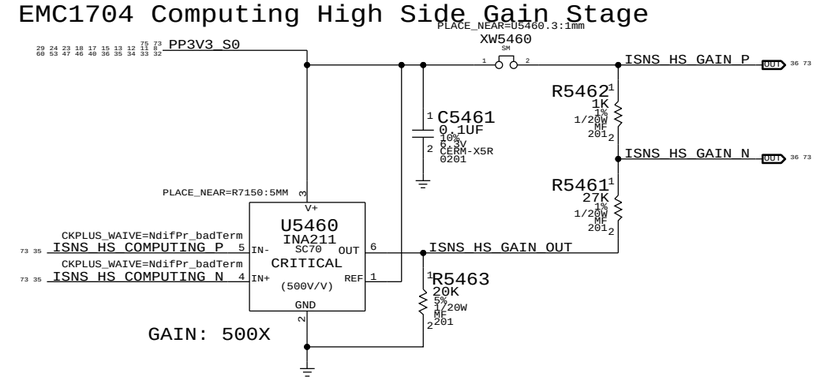


IC0R : COMPUTING High Side Current Sense



Need to set gains for ULX

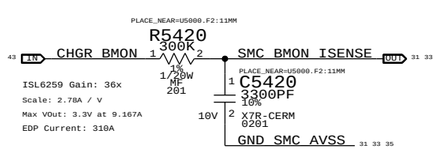
EMC1704 Computing High Side Gain Stage



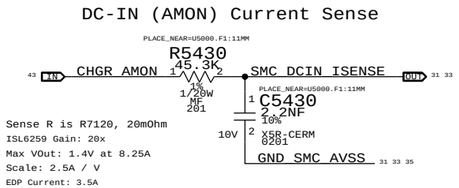
In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800.
This will set the minumum current threshold at 0.100mA

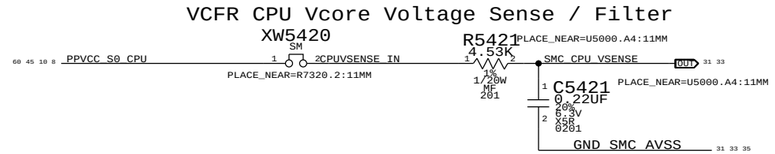
CHARGER BMON High Side Current Sense



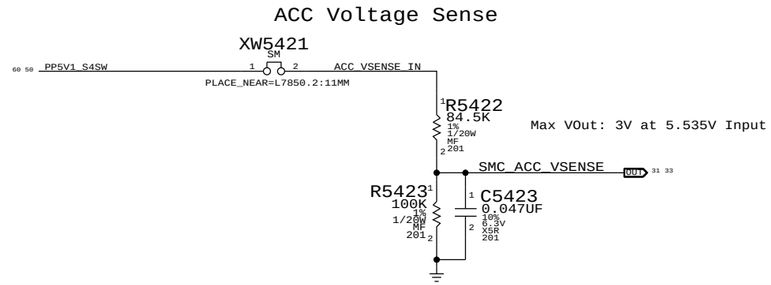
DC-IN (AMON) Current Sense



VCFR CPU Vcore Voltage Sense / Filter



ACC Voltage Sense



SYNC_MASTER=J92_DEVMLB SYNC_DATE=02/07/2014

PAGE TITLE
Voltage & Current Sensing

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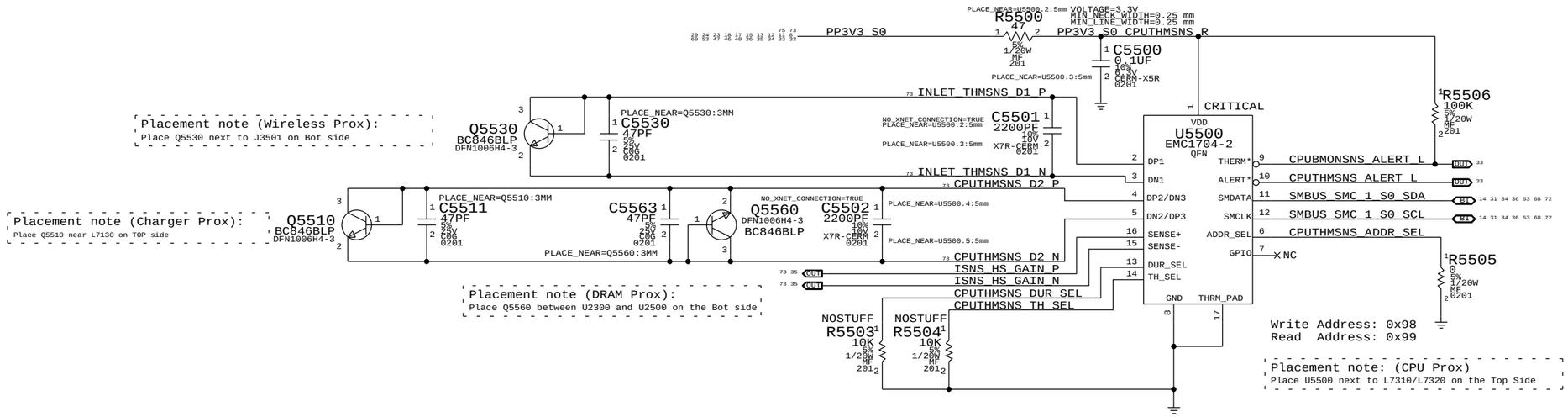
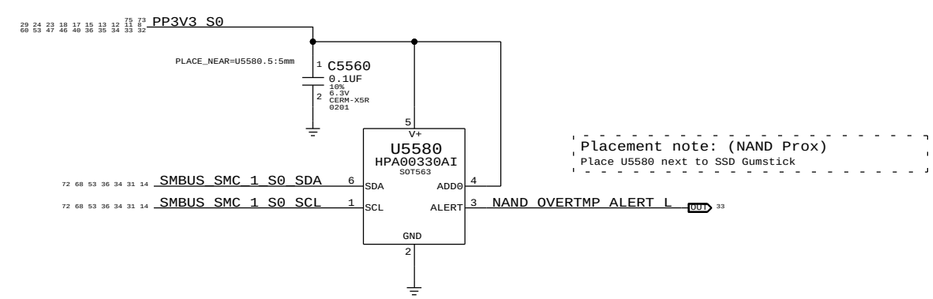
POR THERMAL SENSORS : TO BE USED IN PRODUCTION

CPU Proximity, Inlet ,DDR and BMON THR Sensor



NAND Temp Sensor



SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/12/2013

PAGE TITLE
Temperature Sensing

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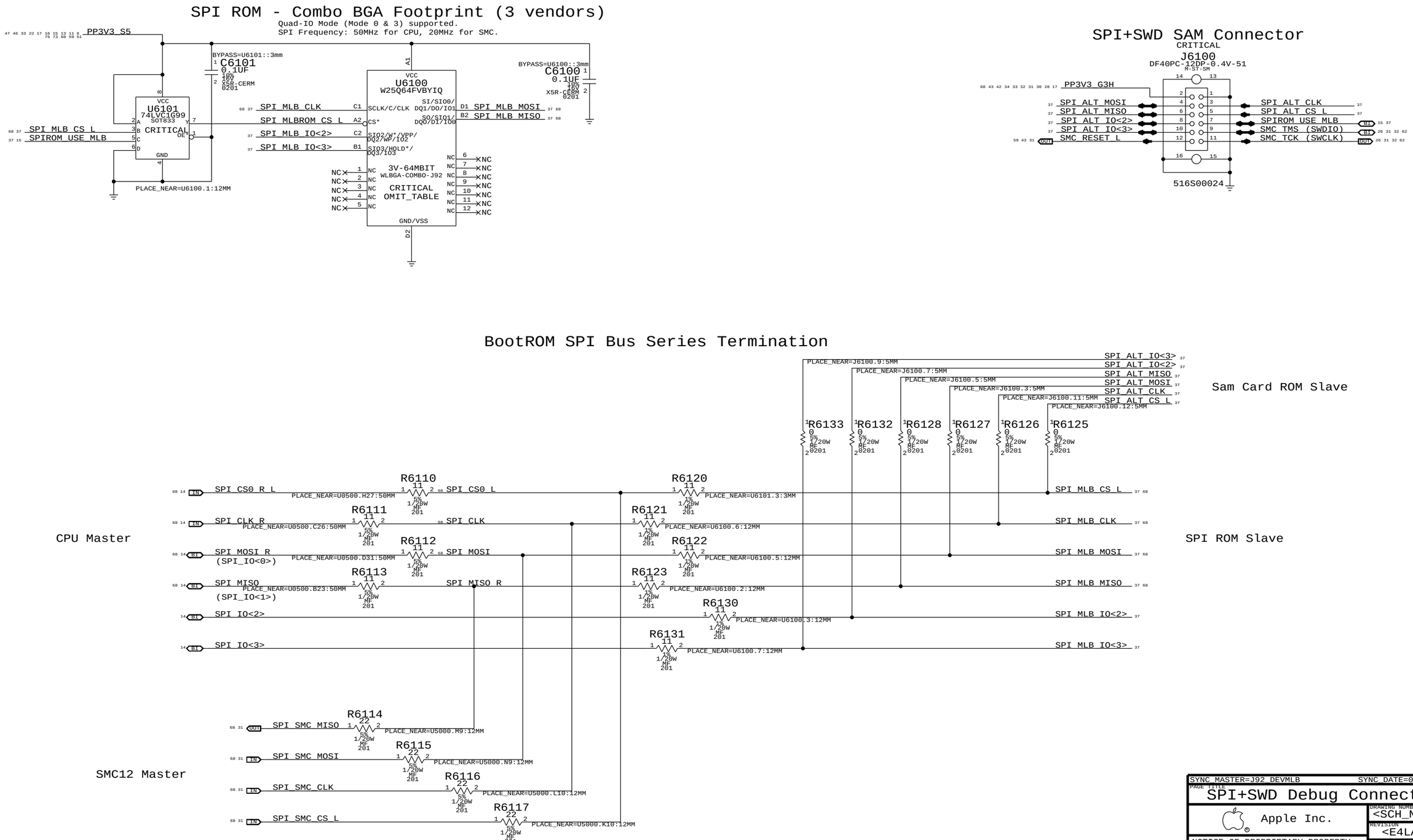

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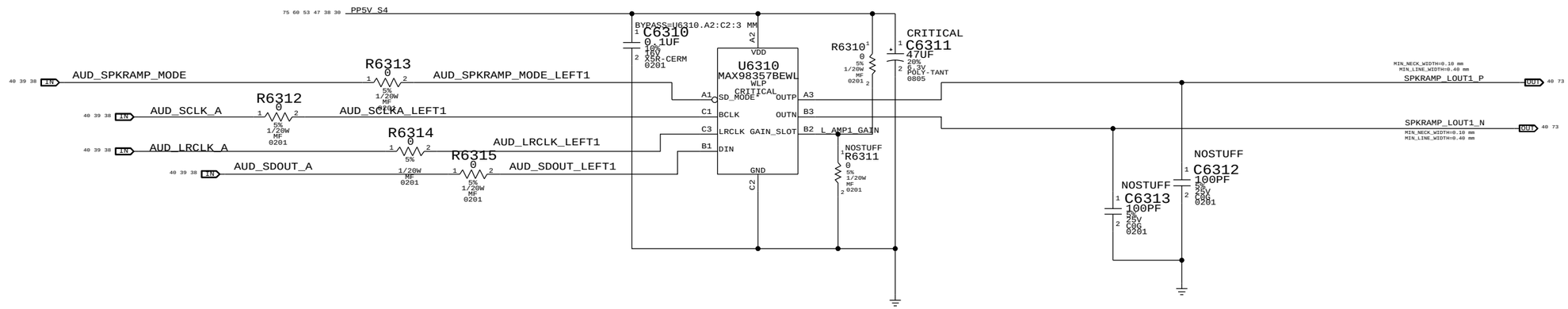
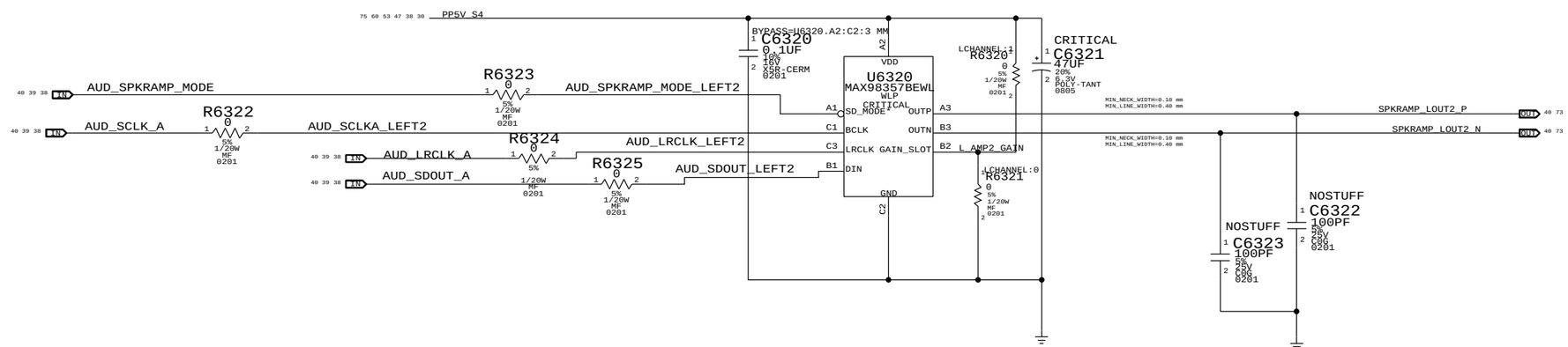
Left Speaker Amps

APPLE P/N 353S4265





SPEAKER CONFIGS

BOM GROUP	BOM OPTIONS
EQ:2CH	LCHANNEL:1,RCHANNEL:3
EQ:4CH	LCHANNEL:0,RCHANNEL:4

SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/19/2013

PAGE TITLE
Audio:Left Speaker Amps

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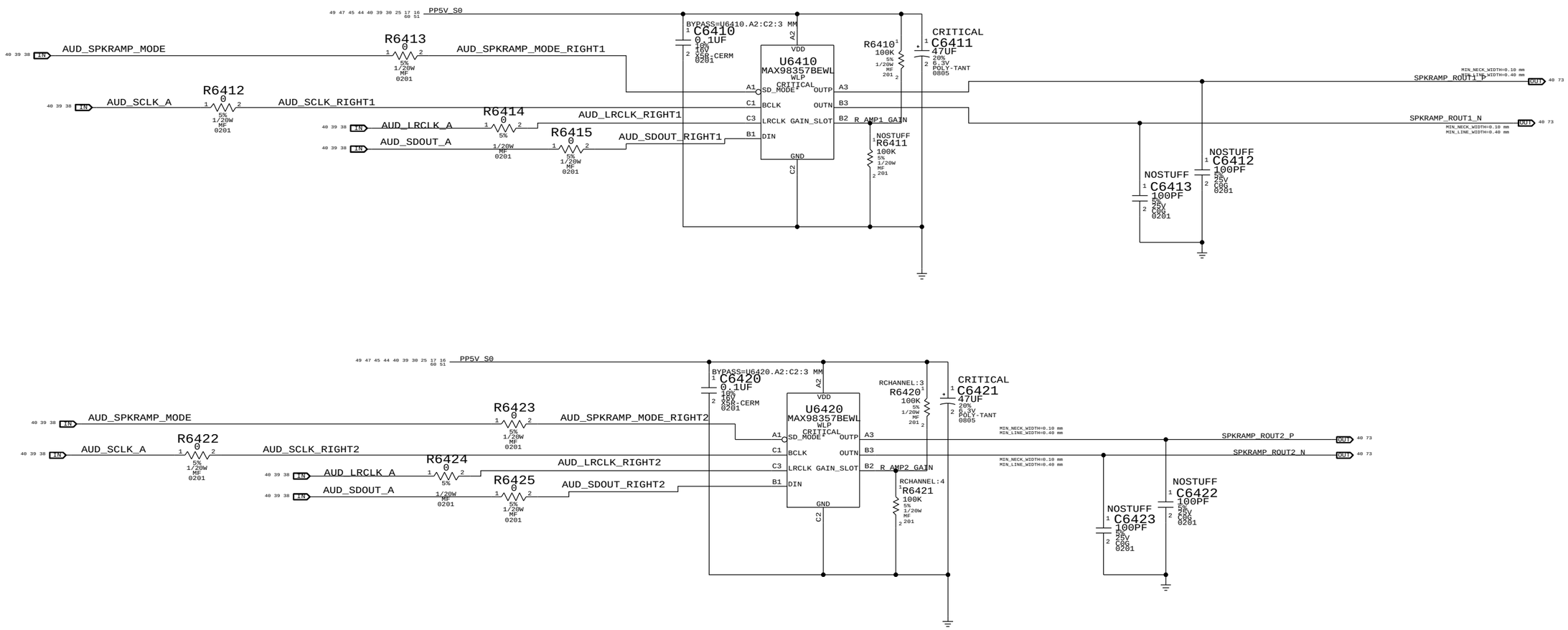
Right Speaker Amps

APPLE P/N 353S4265



SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/19/2013

PAGE TITLE
Audio:Right Speaker Amps

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)		0X09 (A)
SPEAKERS	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A

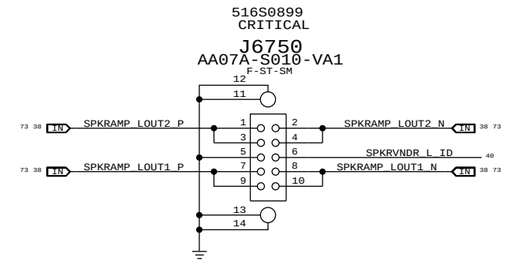
CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

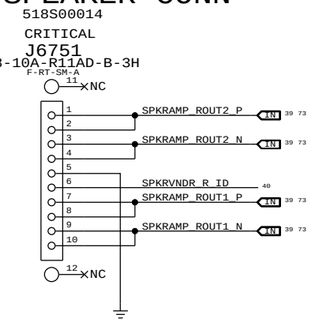
SOUTHBRIDGE RESOURCE/PIN ALLOCATIONS

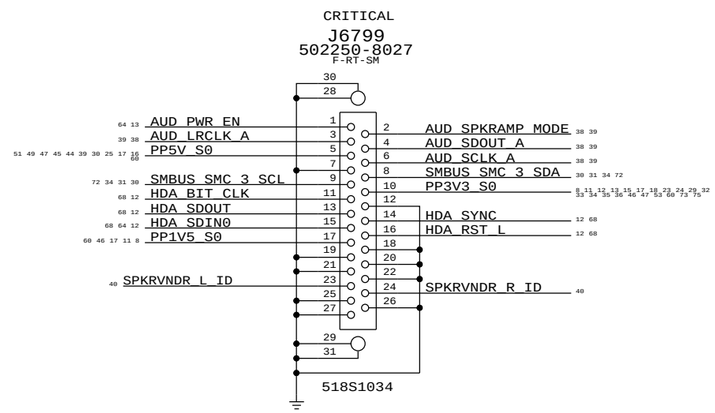
FUNCTION	NET NAME	SB GPIO/INT
PERIPHERAL/EXTRACTION DETECT	AUD_IP_PERIPHERAL_DET	GPIO 3
MIKEY INTERRUPT	AUD_I2C_INT_L	GPIO 5
MIKEY ENABLE	AUD_IPHS_SWITCH_EN	GPIO 16
MIKEY I2C BUS	I2C_MIKEY_SDA/SCL	SMBUS 0

LEFT SPEAKER CONN



RIGHT SPEAKER CONN





RIO FLEX CONN

SYNC_MASTER=CARA_J92 SYNC_DATE=04/17/2014

PAGE TITLE
AUDIO: CONNECTORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 67 OF 130

SHEET 40 OF 75

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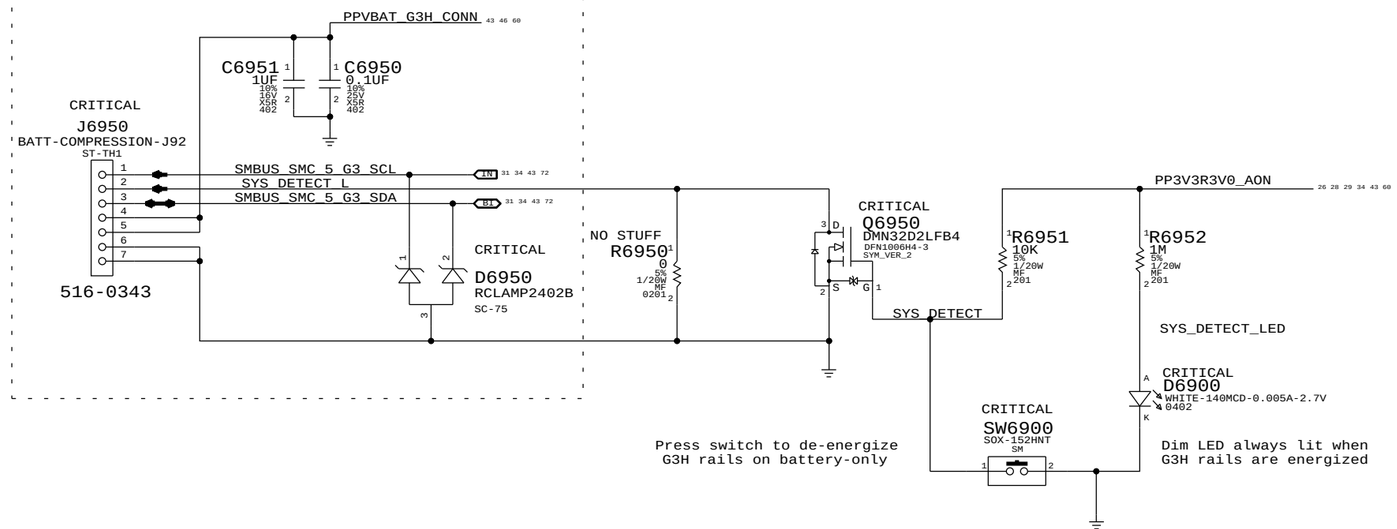
Battery Connector



SYNC MASTER=J43_MLB SYNC DATE=10/24/2012

PAGE TITLE
Battery Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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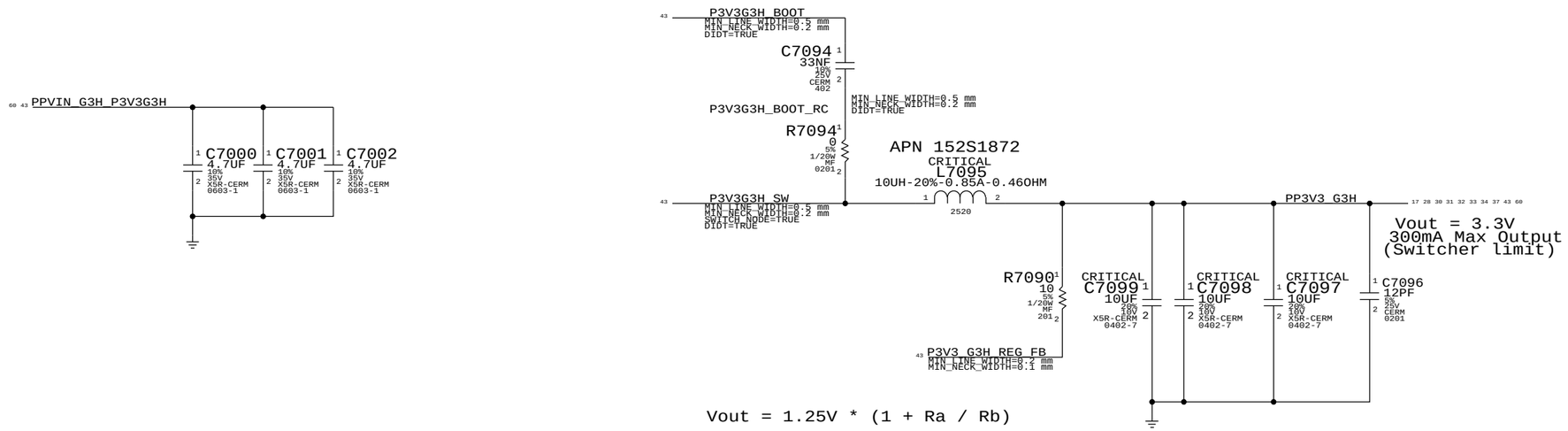
3.3V G3H VR - Bansuri



Vout = 1.25V * (1 + Ra / Rb)

SYNC_MASTER=J92_WILL SYNC_DATE=02/04/2013

PAGE TITLE
3.3V G3Hot Regulator

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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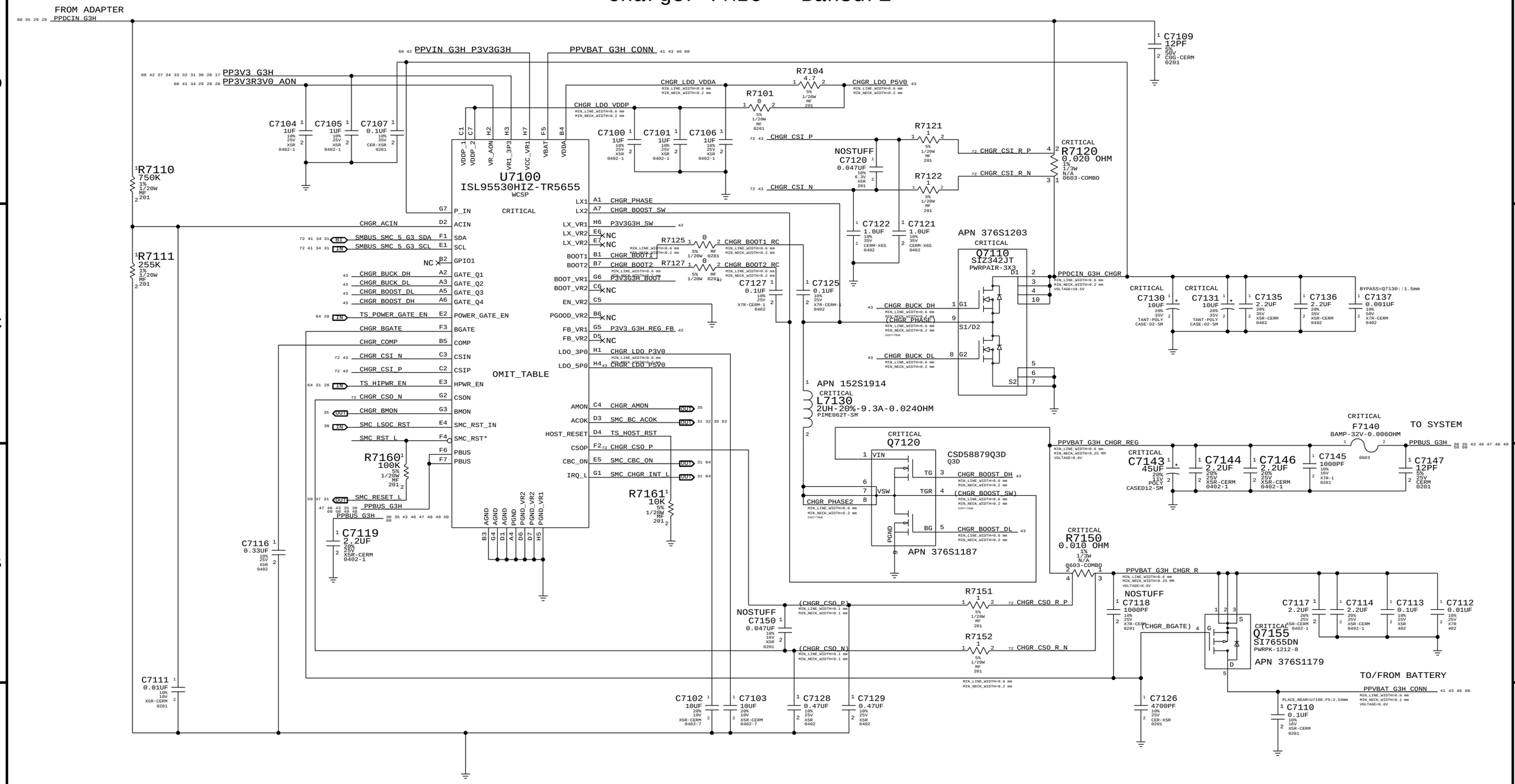
Charger PMIC - Bansuri



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00347	1	IC,ISL95530B1T11,CHGR PMU,BANSURI,WCSP56	U7100	CRITICAL	

SYNC_MASTER=J92_DEVMLB SYNC_DATE=04/04/2014

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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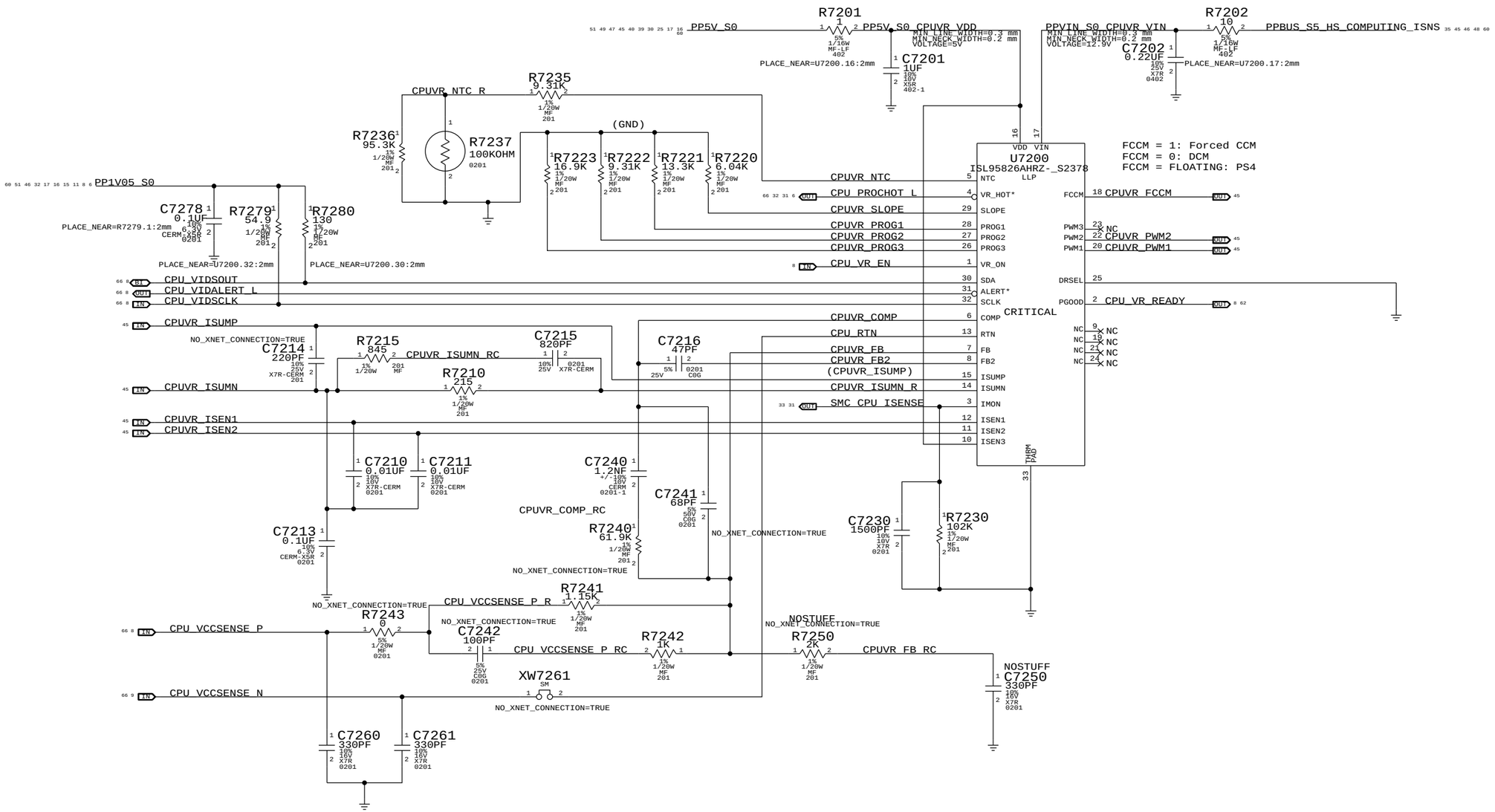

SYNC_MASTER=J43_MLB	SYNC_DATE=10/09/2012
PAGE TITLE: CPU VR12.6 VCC Regulator IC	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
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	PAGE: 72 OF 130
	SHEET: 44 OF 75

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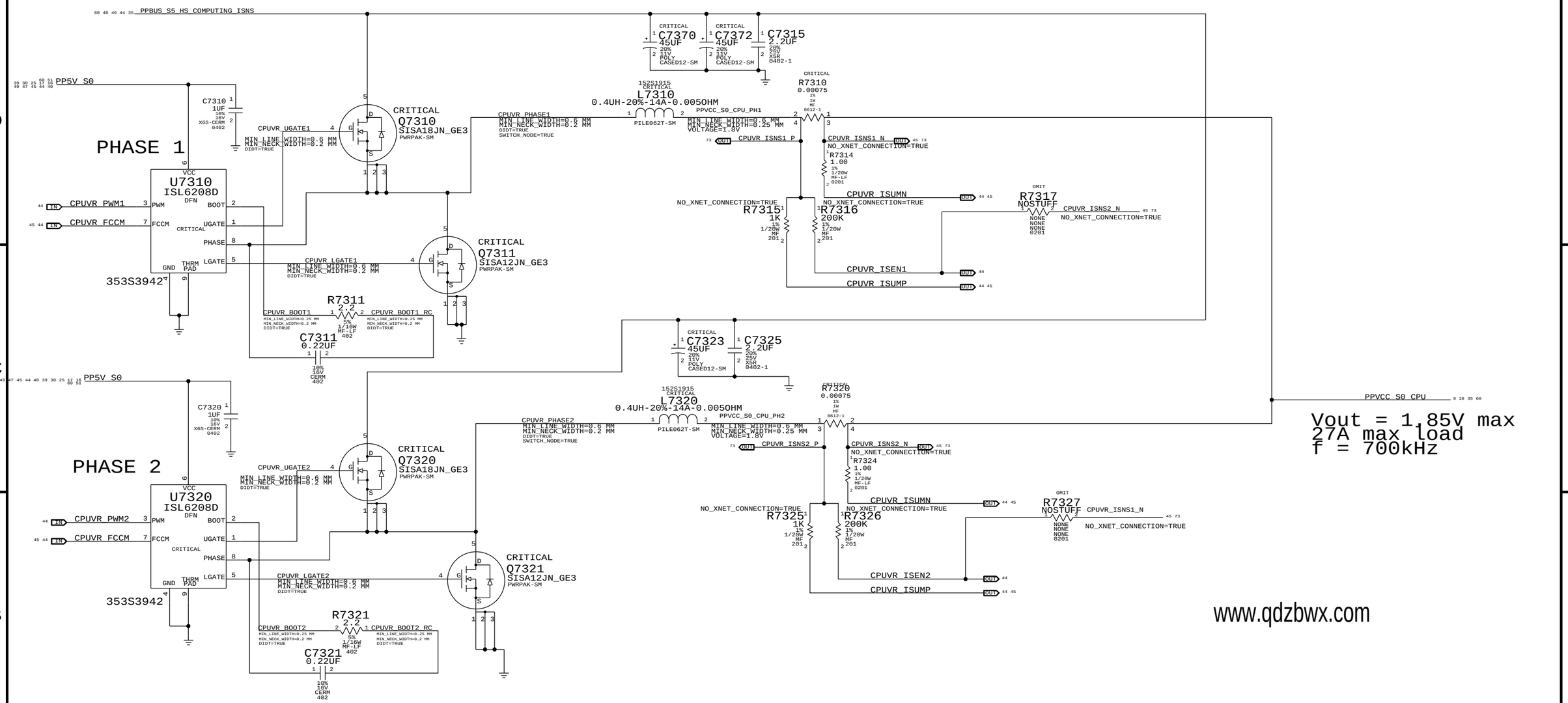

SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014

PAGE TITLE
CPU VR12.5 VCC Power Stage

Apple Inc.

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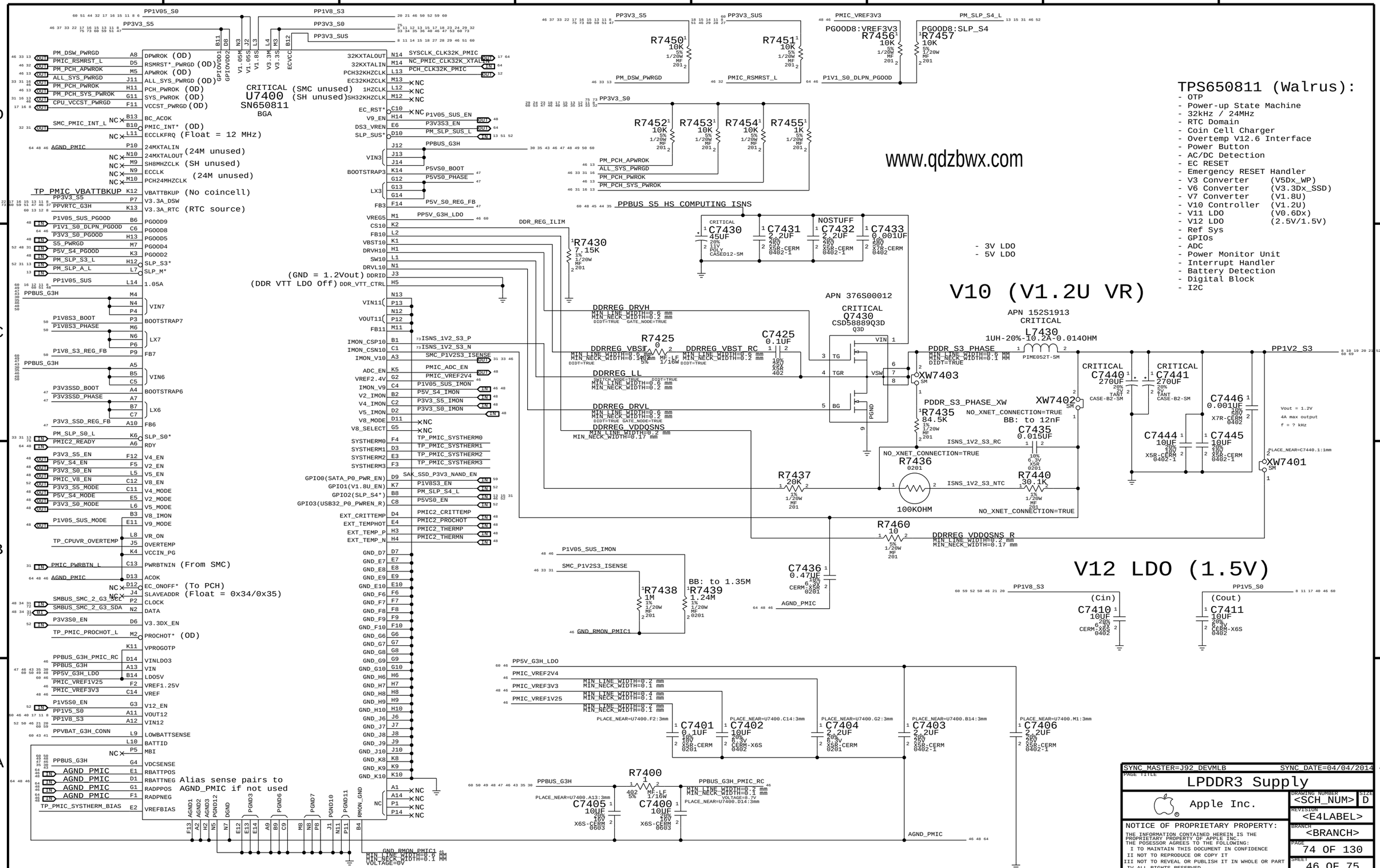

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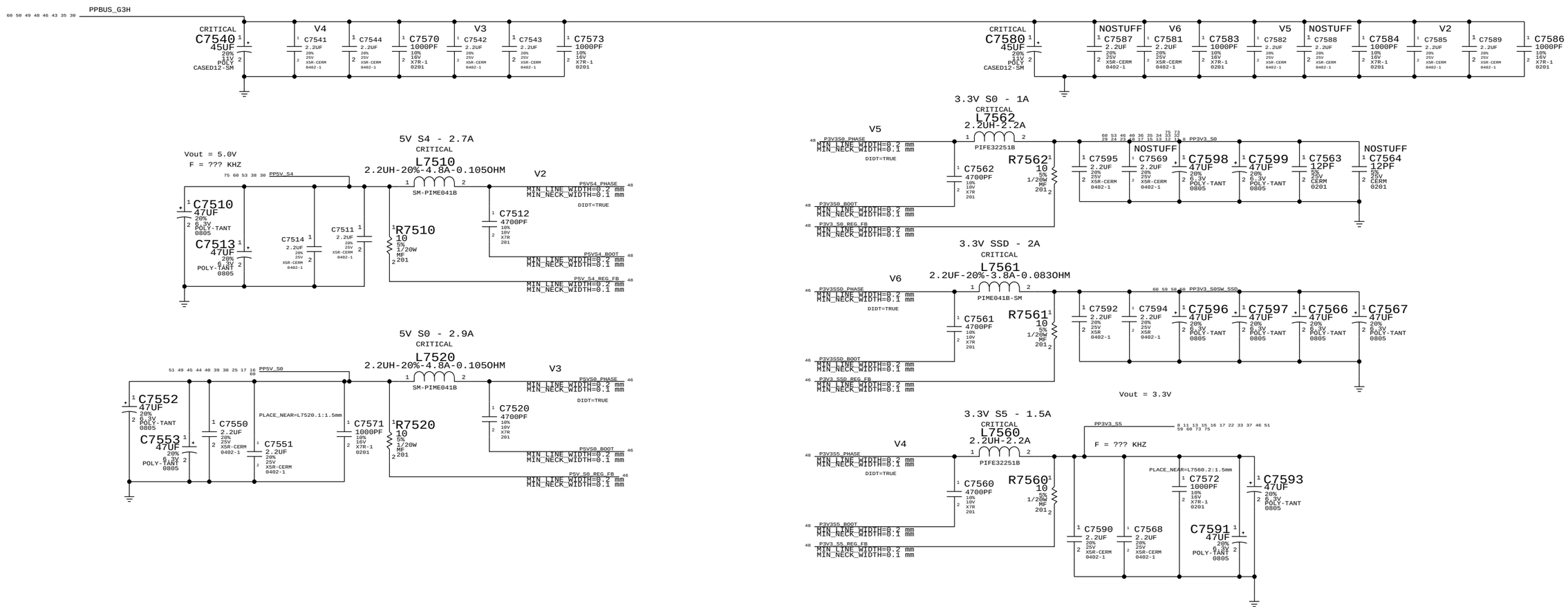

SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014

PAGE TITLE
5V & 3.3V Power Supplies

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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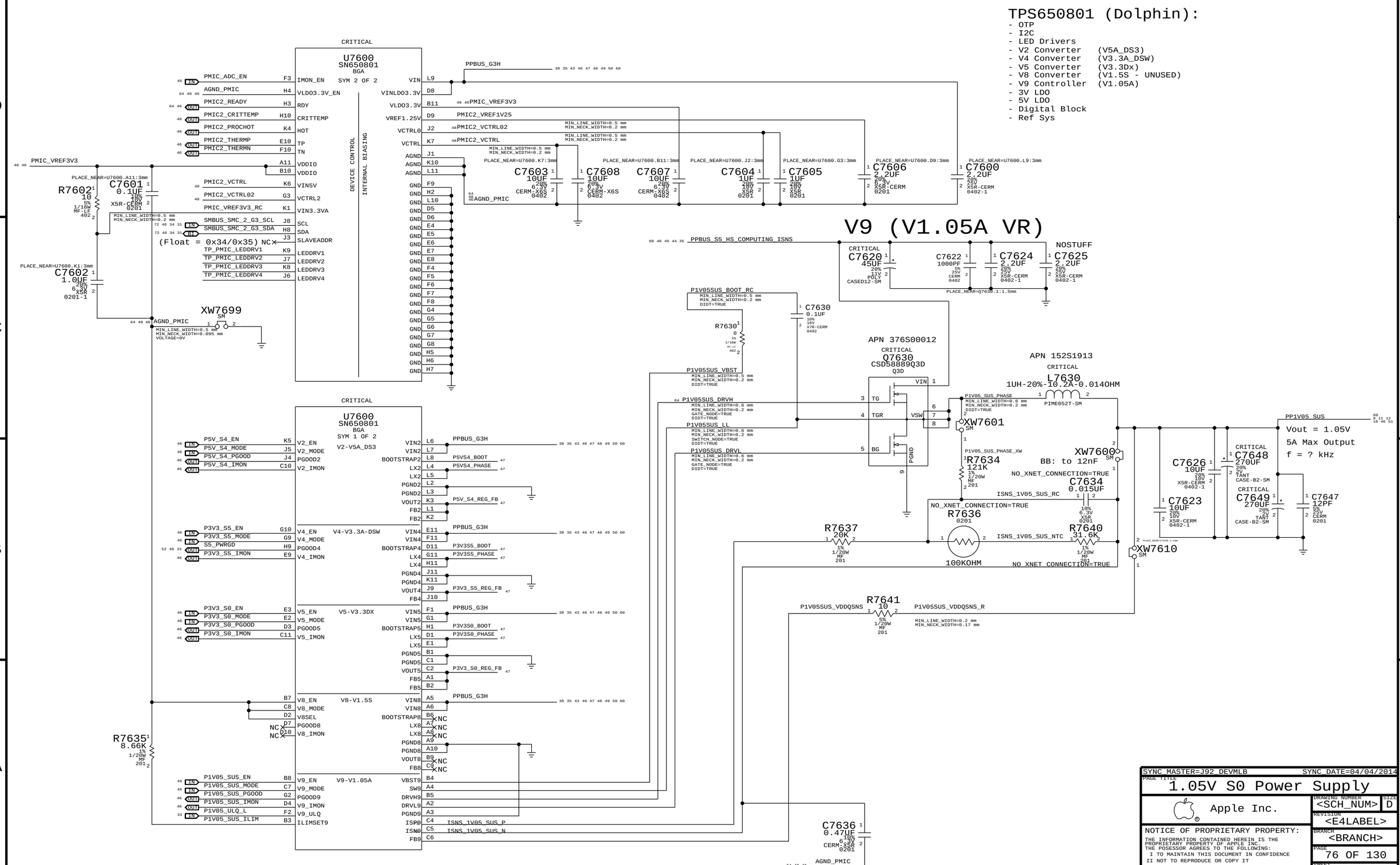

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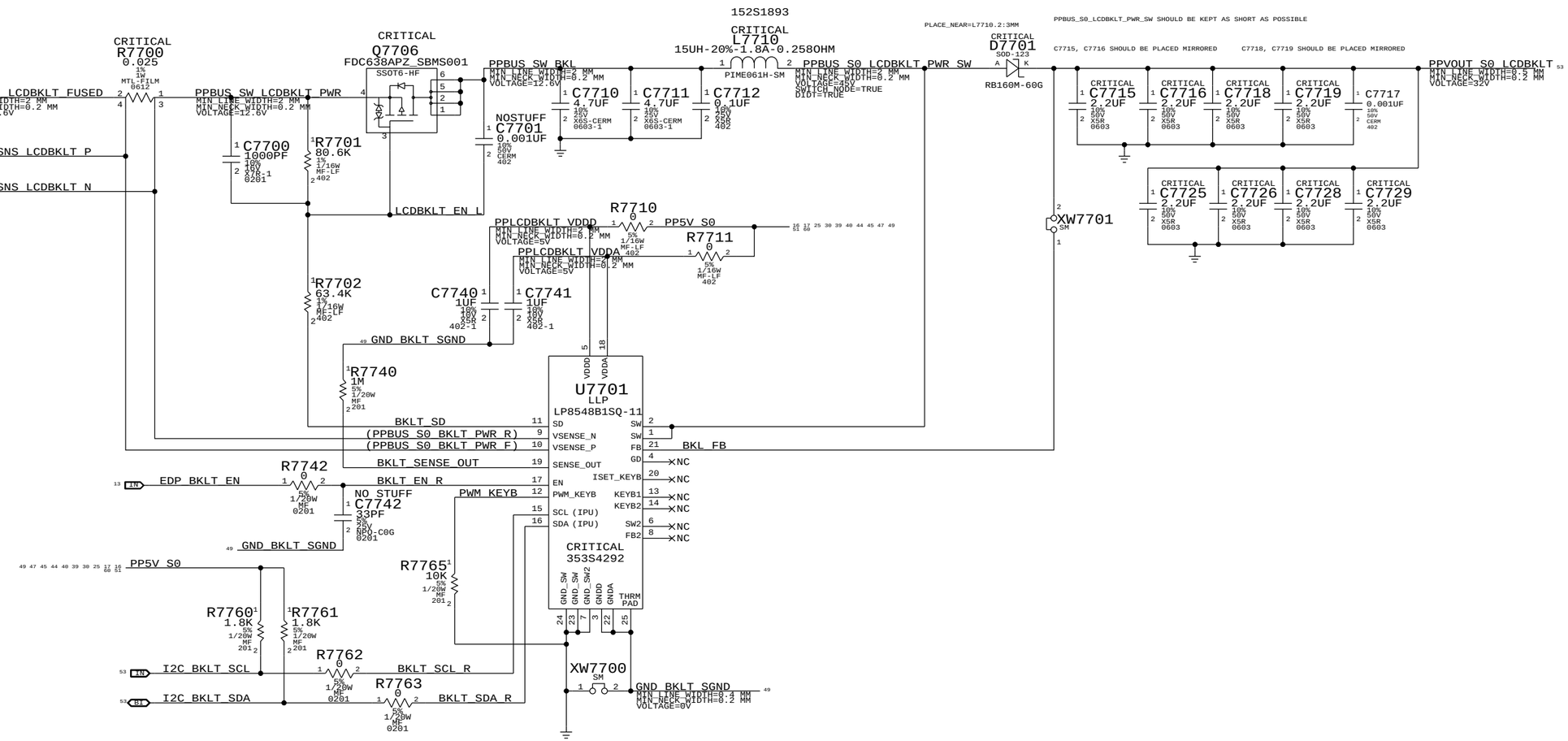
Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (6-8.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production



SYNC_MASTER=J92_DEVMLB SYNC_DATE=10/01/2013

PAGE TITLE
LCD Backlight Driver

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
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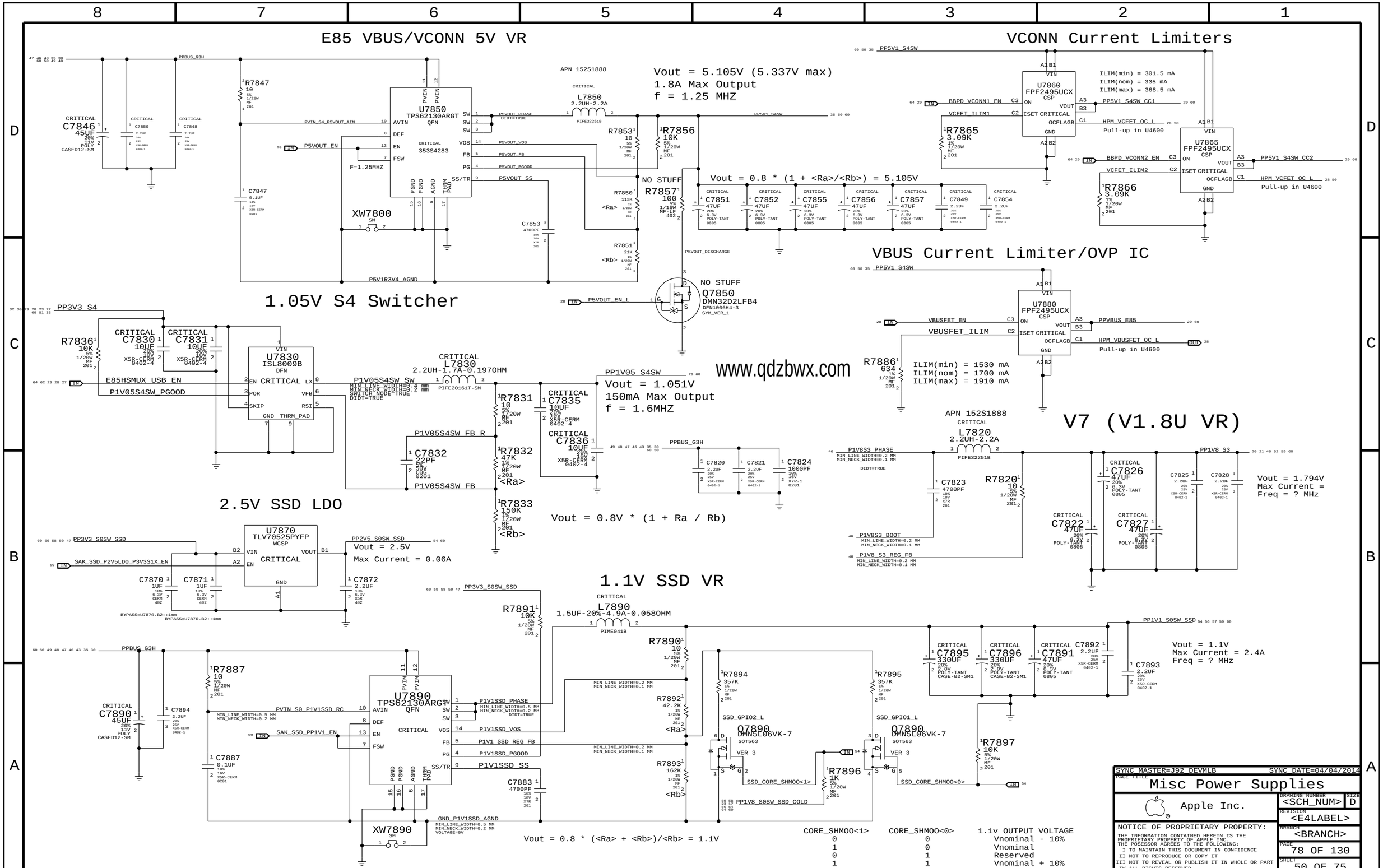

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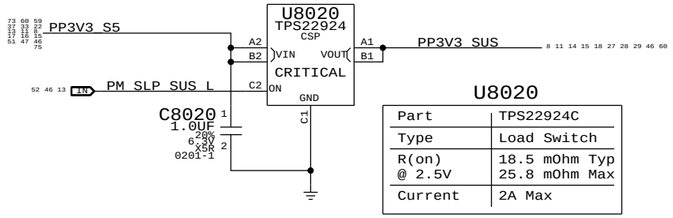
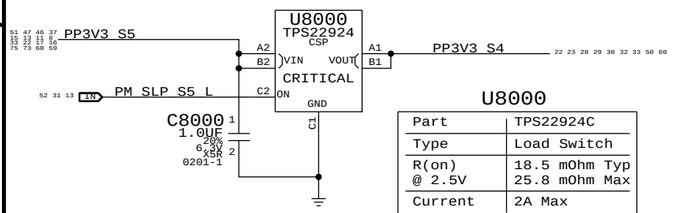
3.3V SUS Switch



U8020

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

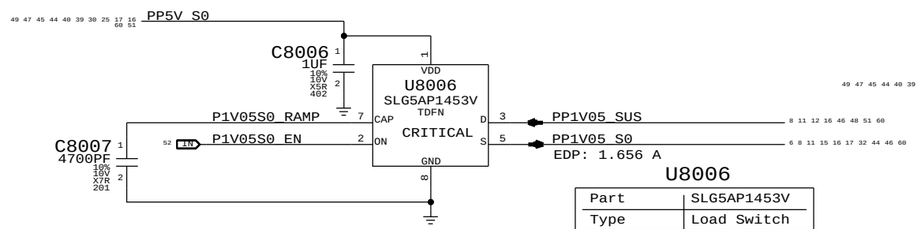
3.3V S4 Switch



U8000

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

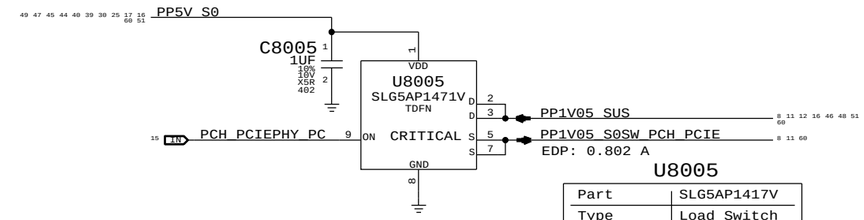
1.05V S0 Switch



U8006

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

1.05V PCH PCIe Switch

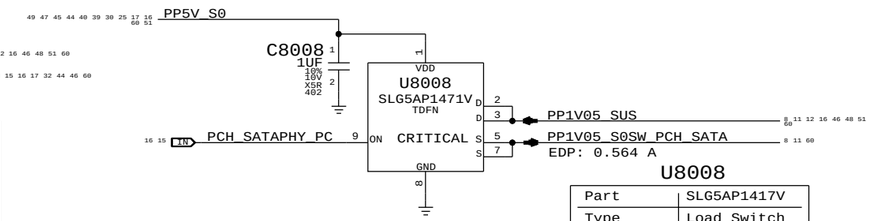


HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

1.05V PCH SATA Switch

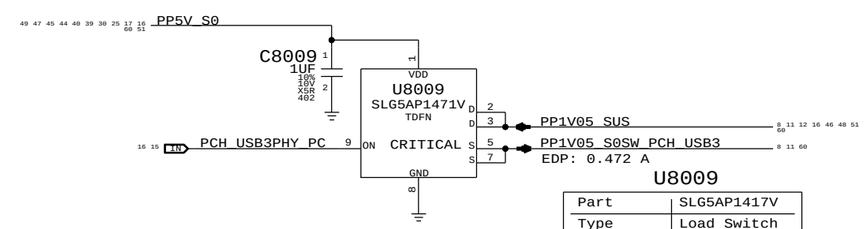


HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

U8008

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

1.05V PCH USB3 Switch



HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

U8009

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

SYNC_MASTER=J92_DEVMLB SYNC_DATE=07/24/2013

PAGE TITLE
Power FETs

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SUS_EN	PM_SLP_SS_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

SUS & S4 Enables

52 51 31 13 IN PM_SLP_S5_L MAKE_BASE=TRUE = PM_SLP_S5_L OUT 13 31 51 52

52 51 46 13 IN PM_SLP_SUS_L MAKE_BASE=TRUE = PM_SLP_SUS_L OUT 13 46 51 52

S3 Enables

46 IN PMIC_V8_EN — R8117 0 5% 1/20W MF 0201

46 31 15 13 IN PM_SLP_S4_L

NO STUFF D8115 0201 RB521ES-30 (A, K)

P1V8S3_EN_D

NO STUFF R8116 30K 5% 1/20W MF 201

NO STUFF R8115 1K 5% 1/20W MF 201

52 46 P1V8S3_EN MAKE_BASE=TRUE = P1V8S3_EN OUT 46 52

NO STUFF C8116 0.1UF 10% 6.3V CERM-X5R 0201

S5 Power Good

52 48 46 31 IN S5_PWRGD = S5_PWRGD MAKE_BASE=TRUE OUT 31 46 48 52

S0 Enables

46 31 13 IN PM_SLP_S3_L

D8182 0201 RB521ES-30 (K, A) — P1V5S0_EN_D — R8182 4.99K 1% 1/20W MF 201 — R8185 30K 5% 1/20W MF 201

D8181 0201 RB521ES-30 (K, A) — P3V3S0_EN_D — R8181 2.0K 5% 1/20W MF 201 — R8186 20K 5% 1/20W MF 201

D8183 0201 RB521ES-30 (A, K) — P1V05S0_EN_D — R8183 1K 5% 1/20W MF 201 — R8184 10K 5% 1/20W MF 201 — R8187 0 5% 1/20W MF 0201

52 46 P5VS0_EN MAKE_BASE=TRUE = P5VS0_EN OUT 46 52

52 51 P1V05S0_EN MAKE_BASE=TRUE = P1V05S0_EN OUT 51 52

52 46 P3V3S0_EN MAKE_BASE=TRUE = P3V3S0_EN OUT 46 52

52 46 P1V5S0_EN MAKE_BASE=TRUE = P1V5S0_EN OUT 46 52

C8185 0.1UF 10% 6.3V CERM-X5R 0201 — C8186 0.1UF 10% 6.3V CERM-X5R 0201 — C8184 0.1UF 10% 6.3V CERM-X5R 0201 — NO STUFF C8187 0.1UF 10% 6.3V CERM-X5R 0201

LPDDR power down sequencing support

NO STUFF D8170 SOD-962 PMEG1201AESF (K, A)

PP1V8_S3 — 20 21 46 50 59 60

PP1V2_S3 — 8 10 19 20 21 46 59 60 69

SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/20/2013

PAGE TITLE: Power Control

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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SHEET: 52 OF 75

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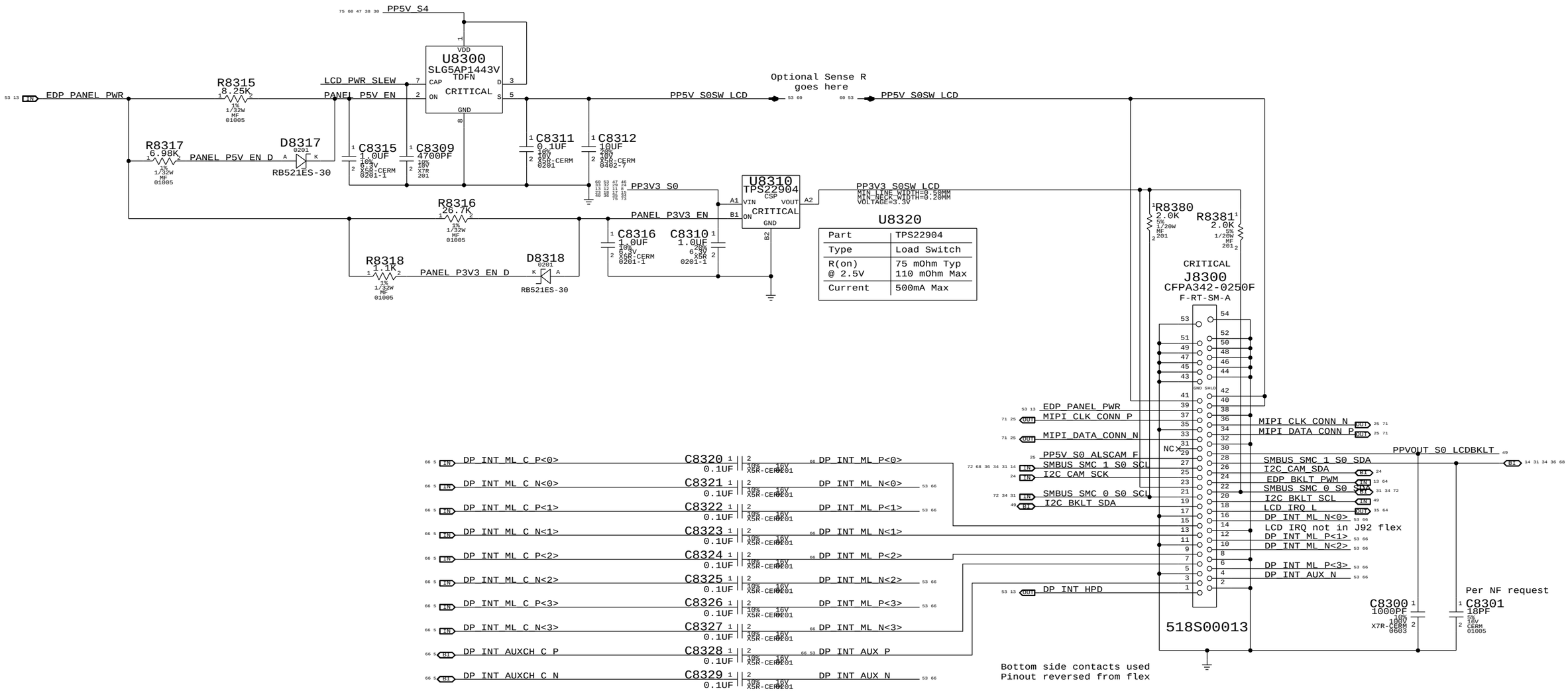
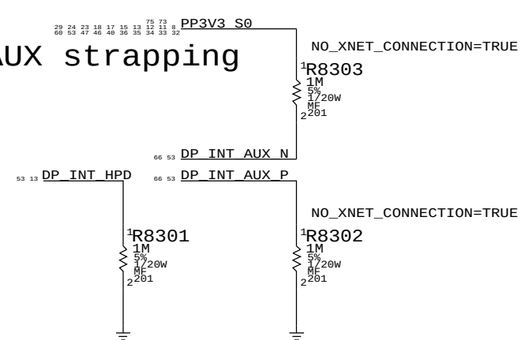
LCD PANEL INTERFACE (eDP) + Camera (MIPI)



U8320

Part	TPS22904
Type	Load Switch
R(on) @ 2.5V	75 mOhm Typ 110 mOhm Max
Current	500mA Max

LCD Panel HPD & AUX strapping



SYNC_MASTER=J92_DEVMLB SYNC_DATE=09/25/2013

PAGE TITLE: eDP Display Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 83 OF 130

SHEET: 53 OF 75

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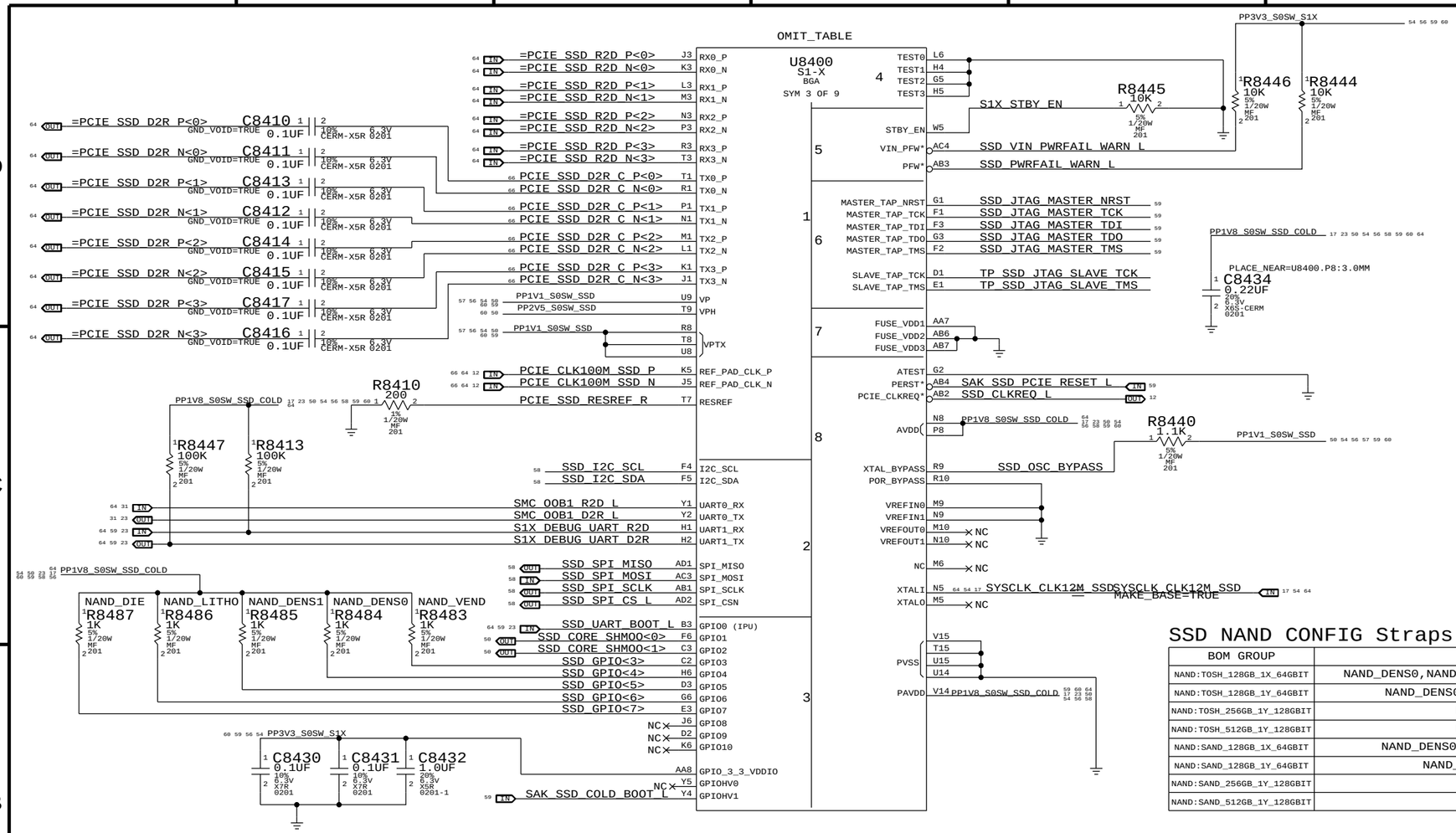

SSD NAND CONFIG Straps

BOM GROUP	BOM OPTIONS
NAND:TOSH_128GB_1X_64GBIT	NAND_DENS0,NAND_DENS1,NAND_VEND,NAND_LITHO,NAND_DIE,NAND_TYPE:TOSH_128GB_1X_64GBIT
NAND:TOSH_128GB_1Y_64GBIT	NAND_DENS0,NAND_DENS1,NAND_VEND,NAND_DIE,NAND_TYPE:TOSH_128GB_1Y_64GBIT
NAND:TOSH_256GB_1Y_128GBIT	NAND_VEND,NAND_DENS1,NAND_TYPE:TOSH_256GB_1Y_128GBIT
NAND:TOSH_512GB_1Y_128GBIT	NAND_VEND,NAND_DENS0,NAND_TYPE:TOSH_512GB_1Y_128GBIT
NAND:SAND_128GB_1X_64GBIT	NAND_DENS0,NAND_DENS1,NAND_LITHO,NAND_DIE,NAND_TYPE:SAND_128GB_1X_64GBIT
NAND:SAND_128GB_1Y_64GBIT	NAND_DENS0,NAND_DENS1,NAND_DIE,NAND_TYPE:SAND_128GB_1Y_64GBIT
NAND:SAND_256GB_1Y_128GBIT	NAND_DENS1,NAND_TYPE:SAND_256GB_1Y_128GBIT
NAND:SAND_512GB_1Y_128GBIT	NAND_DENS0,NAND_TYPE:SAND_512GB_1Y_128GBIT

S1-X GPIO[10:1] IPD

VENDOR	NAND_VEND(GPIO3)
TOSHIBA	1
SANDISK	0

DENSITY	NAND_DENS0(GPIO4)	NAND_DENS1(GPIO5)
128GB	1	1
256GB	0	1
512GB	1	0

LITHO	NAND_LITHO(GPIO6)
1X	1
1Y	0

DIE SIZE	NAND_DIE(GPIO7)
64Gb	1
128Gb	0

# NAND_CH	(GPIO8)
8 (X56)	1
4 (J92)	0

SSD NAND Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-7360	2	NAND,19NM,64GX8,MLC,RAW,64G,2-CH,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_128GB_1X_64GBIT
335S00004	2	NAND,TOGGLE DDR2,2CH,64GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_128GB_1Y_64GBIT
335S1031	2	NAND,TOGGLE DDR2,2CH,128GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_256GB_1Y_128GBIT
335S1032	2	NAND,TOGGLE DDR2,2CH,256GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:TOSH_512GB_1Y_128GBIT
998-7361	2	NAND,19NM,64GX8,MLC,RAW,64G,2-CH,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_128GB_1X_64GBIT
335S1044	2	NAND,TOGGLE DDR2,2CH,64GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_128GB_1Y_64GBIT
335S1041	2	NAND,TOGGLE DDR2,2CH,128GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_256GB_1Y_128GBIT
335S1045	2	NAND,TOGGLE DDR2,2CH,256GB,1YNM,3.3V,LGA60	U8801,U8810	CRITICAL	NAND_TYPE:SAND_512GB_1Y_128GBIT

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70 58 OUT	ANI0_ALE	F18	ANI0_ALE		ANI2_ALE	E12	NC
70 58 OUT	ANI0_CLE	D19	ANI0_CLE		ANI2_CLE	D11	NC
70 58 BI	ANI0_DQS_N	B20	ANI0_DQS_N		ANI2_DQS_N	B14	NC
70 58 BI	ANI0_DQS_P	A20	ANI0_DQS_P		ANI2_DQS_P	A14	NC
70 58 BI	ANI0_IO<0>	B22	ANI0_IO0		ANI2_IO0	A16	NC
70 58 BI	ANI0_IO<1>	A23	ANI0_IO1		ANI2_IO1	A11	NC
70 58 BI	ANI0_IO<2>	B21	ANI0_IO2		ANI2_IO2	B16	NC
70 58 BI	ANI0_IO<3>	A22	ANI0_IO3		ANI2_IO3	B11	NC
70 58 BI	ANI0_IO<4>	A21	ANI0_IO4		ANI2_IO4	A12	NC
70 58 BI	ANI0_IO<5>	B18	ANI0_IO5		ANI2_IO5	B12	NC
70 58 BI	ANI0_IO<6>	A18	ANI0_IO6		ANI2_IO6	B15	NC
70 58 BI	ANI0_IO<7>	C18	ANI0_IO7	0 2	ANI2_IO7	A15	NC
70 58 OUT	ANI0_NCE<0>	E23	ANI0_NCE0		ANI2_NCE0	E16	NC
70 58 OUT	ANI0_NCE<1>	D22	ANI0_NCE1		ANI2_NCE1	D15	NC
70 58 OUT	ANI0_NCE<2>	E22	ANI0_NCE2		ANI2_NCE2	E15	NC
70 58 OUT	ANI0_NCE<3>	D21	ANI0_NCE3		ANI2_NCE3	D14	NC
NC		E21	ANI0_NCE4		ANI2_NCE4	E14	NC
NC		D20	ANI0_NCE5		ANI2_NCE5	D13	NC
NC		E20	ANI0_NCE6		ANI2_NCE6	E13	NC
NC		E19	ANI0_NCE7		ANI2_NCE7	D12	NC
70 58 BI	ANI0_NRE_N	B19	ANI0_NRE_N		ANI2_NRE_N	B13	NC
70 58 BI	ANI0_NRE_P	A19	ANI0_NRE_P		ANI2_NRE_P	A13	NC
70 58 OUT	ANI0_NWE	D23	ANI0_NWE		ANI2_NWE	D16	NC
NC		D18	ANI0_PPM_IN		ANI2_PPM_IN	E11	NC
NC		E18	ANI0_PPM_OUT		ANI2_PPM_OUT	F11	NC
70 58 OUT	ANI1_ALE	D25	ANI1_ALE		ANI3_ALE	D5	NC
70 58 OUT	ANI1_CLE	D26	ANI1_CLE		ANI3_CLE	E5	NC
70 58 BI	ANI1_DQS_N	E28	ANI1_DQS_N		ANI3_DQS_N	B6	NC
70 58 BI	ANI1_DQS_P	E29	ANI1_DQS_P		ANI3_DQS_P	A6	NC
70 58 BI	ANI1_IO<0>	G28	ANI1_IO0		ANI3_IO0	B4	NC
70 58 BI	ANI1_IO<1>	J29	ANI1_IO1		ANI3_IO1	A7	NC
70 58 BI	ANI1_IO<2>	G29	ANI1_IO2		ANI3_IO2	C4	NC
70 58 BI	ANI1_IO<3>	L29	ANI1_IO3		ANI3_IO3	B9	NC
70 58 BI	ANI1_IO<4>	J28	ANI1_IO4		ANI3_IO4	B8	NC
70 58 BI	ANI1_IO<5>	B26	ANI1_IO5		ANI3_IO5	A9	NC
70 58 BI	ANI1_IO<6>	C26	ANI1_IO6		ANI3_IO6	A4	NC
70 58 BI	ANI1_IO<7>	B25	ANI1_IO7	1 3	ANI3_IO7	A8	NC
70 58 OUT	ANI1_NCE<0>	J25	ANI1_NCE0		ANI3_NCE0	D9	NC
70 58 OUT	ANI1_NCE<1>	J26	ANI1_NCE1		ANI3_NCE1	E9	NC
70 58 OUT	ANI1_NCE<2>	H25	ANI1_NCE2		ANI3_NCE2	D8	NC
70 58 OUT	ANI1_NCE<3>	H26	ANI1_NCE3		ANI3_NCE3	E8	NC
NC		G25	ANI1_NCE4		ANI3_NCE4	D7	NC
NC		G26	ANI1_NCE5		ANI3_NCE5	E7	NC
NC		F25	ANI1_NCE6		ANI3_NCE6	D6	NC
NC		F26	ANI1_NCE7		ANI3_NCE7	E6	NC
70 58 BI	ANI1_NRE_N	D27	ANI1_NRE_N		ANI3_NRE_N	B5	NC
70 58 BI	ANI1_NRE_P	C27	ANI1_NRE_P		ANI3_NRE_P	A5	NC
70 58 OUT	ANI1_NWE	K25	ANI1_NWE		ANI3_NWE	F9	NC
NC		E26	ANI1_PPM_IN		ANI3_PPM_IN	D4	NC
NC		E25	ANI1_PPM_OUT		ANI3_PPM_OUT	E4	NC

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NC	AE12	ANI4_ALE		ANI6_ALE	AF25	ANI6_ALE	70 58 OUT
NC	AF11	ANI4_CLE		ANI6_CLE	AF26	ANI6_CLE	70 58 OUT
NC	AH14	ANI4_DQS_N		ANI6_DQS_N	AE28	ANI6_DQS_N	70 58 BI
NC	AJ14	ANI4_DQS_P		ANI6_DQS_P	AE29	ANI6_DQS_P	70 58 BI
NC	AJ11	ANI4_IO0		ANI6_IO0	W29	ANI6_IO<0>	70 58 BI
NC	AJ16	ANI4_IO1		ANI6_IO1	AC29	ANI6_IO<1>	70 58 BI
NC	AH11	ANI4_IO2		ANI6_IO2	AA28	ANI6_IO<2>	70 58 BI
NC	AH16	ANI4_IO3		ANI6_IO3	AG26	ANI6_IO<3>	70 58 BI
NC	AJ15	ANI4_IO4	4 6	ANI6_IO4	AH26	ANI6_IO<4>	70 58 BI
NC	AH15	ANI4_IO5		ANI6_IO5	AH25	ANI6_IO<5>	70 58 BI
NC	AJ12	ANI4_IO6		ANI6_IO6	AA29	ANI6_IO<6>	70 58 BI
NC	AH12	ANI4_IO7		ANI6_IO7	AC28	ANI6_IO<7>	70 58 BI
NC	AE16	ANI4_NCE0		ANI6_NCE0	AA25	ANI6_NCE<0>	70 58 OUT
NC	AF15	ANI4_NCE1		ANI6_NCE1	AA26	ANI6_NCE<1>	70 58 OUT
NC	AE15	ANI4_NCE2		ANI6_NCE2	AB25	ANI6_NCE<2>	70 58 OUT
NC	AF14	ANI4_NCE3		ANI6_NCE3	AB26	ANI6_NCE<3>	70 58 OUT
NC	AE14	ANI4_NCE4		ANI6_NCE4	AC25	NC	
NC	AF13	ANI4_NCE5		ANI6_NCE5	AC26	NC	
NC	AE13	ANI4_NCE6		ANI6_NCE6	AD25	NC	
NC	AF12	ANI4_NCE7		ANI6_NCE7	AD26	NC	
NC	AH13	ANI4_NRE_N		ANI6_NRE_N	AF27	ANI6_NRE_N	70 58 BI
NC	AJ13	ANI4_NRE_P		ANI6_NRE_P	AG27	ANI6_NRE_P	70 58 BI
NC	AF16	ANI4_NWE		ANI6_NWE	W25	ANI6_NWE	70 58 OUT
NC	AE11	ANI4_PPM_IN		ANI6_PPM_IN	AE26	NC	
NC	AD11	ANI4_PPM_OUT		ANI6_PPM_OUT	AE25	NC	
NC	AF5	ANI5_ALE		ANI7_ALE	AD18	ANI7_ALE	70 58 OUT
NC	AE5	ANI5_CLE		ANI7_CLE	AF19	ANI7_CLE	70 58 OUT
NC	AH7	ANI5_DQS_N		ANI7_DQS_N	AH21	ANI7_DQS_N	70 58 BI
NC	AJ7	ANI5_DQS_P		ANI7_DQS_P	AJ21	ANI7_DQS_P	70 58 BI
NC	AH5	ANI5_IO0		ANI7_IO0	AJ23	ANI7_IO<0>	70 58 BI
NC	AJ8	ANI5_IO1		ANI7_IO1	AH23	ANI7_IO<1>	70 58 BI
NC	AH4	ANI5_IO2		ANI7_IO2	AH22	ANI7_IO<2>	70 58 BI
NC	AH8	ANI5_IO3		ANI7_IO3	AJ22	ANI7_IO<3>	70 58 BI
NC	AJ9	ANI5_IO4	5 7	ANI7_IO4	AJ19	ANI7_IO<4>	70 58 BI
NC	AH9	ANI5_IO5		ANI7_IO5	AH19	ANI7_IO<5>	70 58 BI
NC	AJ4	ANI5_IO6		ANI7_IO6	AJ18	ANI7_IO<6>	70 58 BI
NC	AJ5	ANI5_IO7		ANI7_IO7	AH18	ANI7_IO<7>	70 58 BI
NC	AF9	ANI5_NCE0		ANI7_NCE0	AE23	ANI7_NCE<0>	70 58 OUT
NC	AE9	ANI5_NCE1		ANI7_NCE1	AF22	ANI7_NCE<1>	70 58 OUT
NC	AF8	ANI5_NCE2		ANI7_NCE2	AE22	ANI7_NCE<2>	70 58 OUT
NC	AE8	ANI5_NCE3		ANI7_NCE3	AF21	ANI7_NCE<3>	70 58 OUT
NC	AF7	ANI5_NCE4		ANI7_NCE4	AE21	NC	
NC	AE7	ANI5_NCE5		ANI7_NCE5	AF20	NC	
NC	AF6	ANI5_NCE6		ANI7_NCE6	AE20	NC	
NC	AE6	ANI5_NCE7		ANI7_NCE7	AE19	NC	
NC	AH6	ANI5_NRE_N		ANI7_NRE_N	AH20	ANI7_NRE_N	70 58 BI
NC	AJ6	ANI5_NRE_P		ANI7_NRE_P	AJ20	ANI7_NRE_P	70 58 BI
NC	AD9	ANI5_NWE		ANI7_NWE	AF23	ANI7_NWE	70 58 OUT
NC	AF4	ANI5_PPM_IN		ANI7_PPM_IN	AF18	NC	
NC	AE4	ANI5_PPM_OUT		ANI7_PPM_OUT	AE18	NC	

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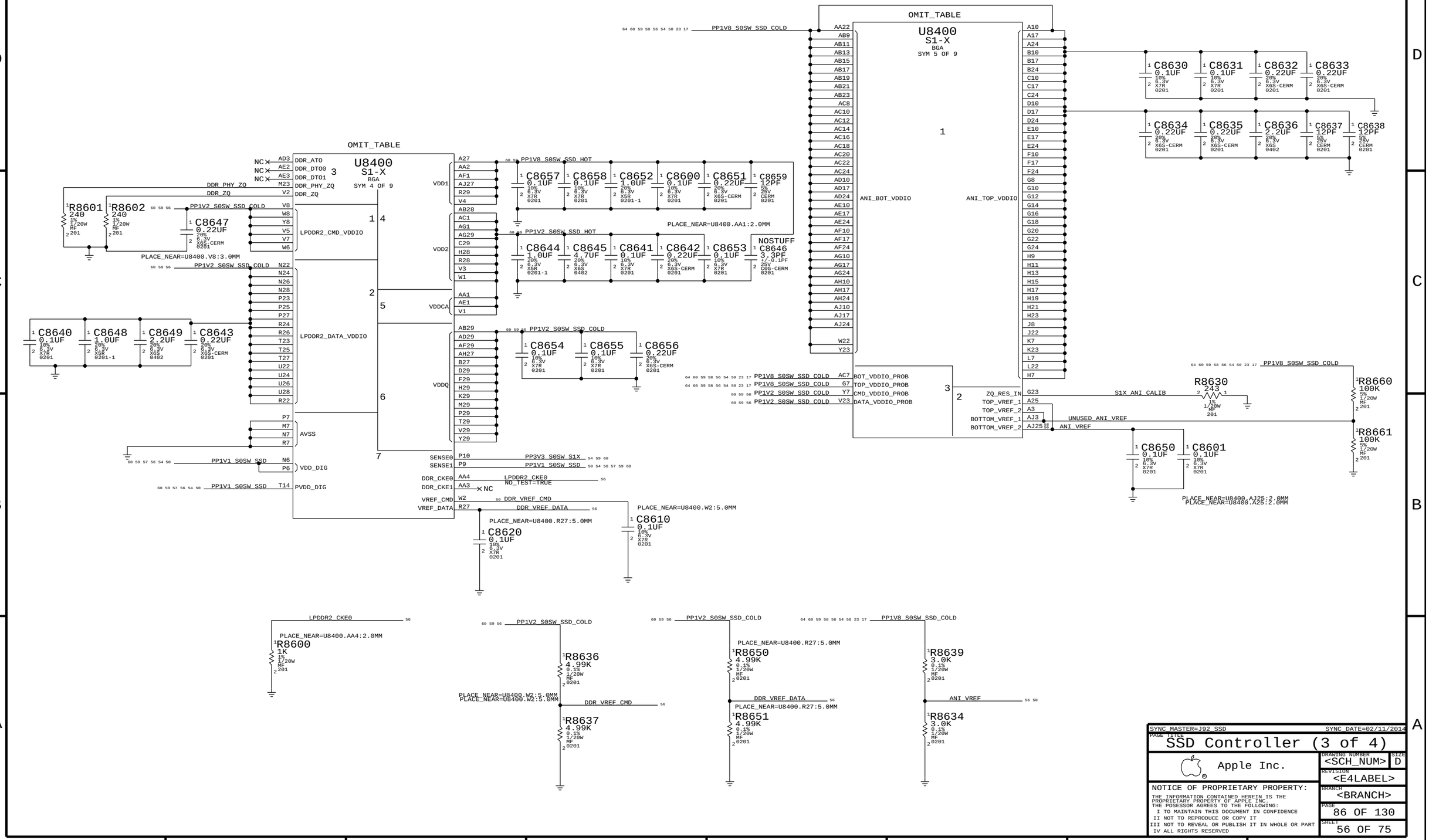

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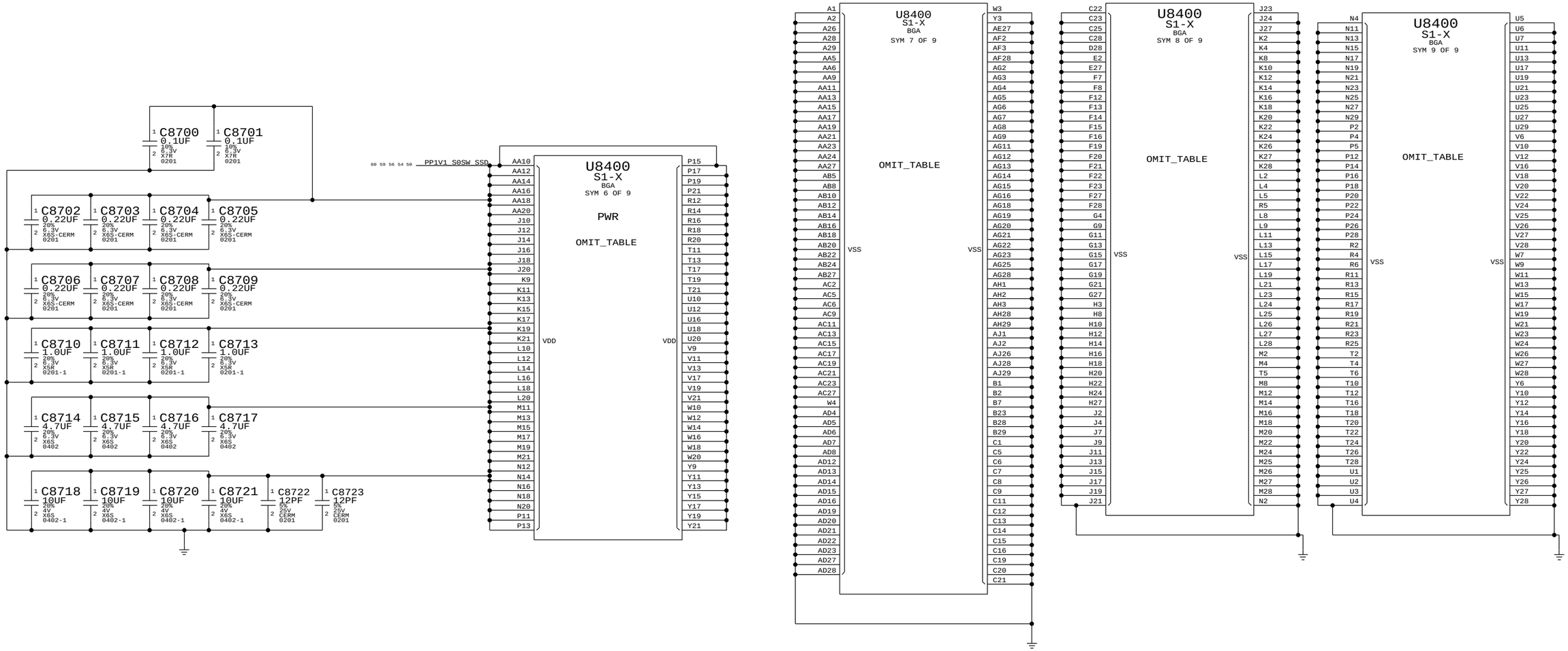

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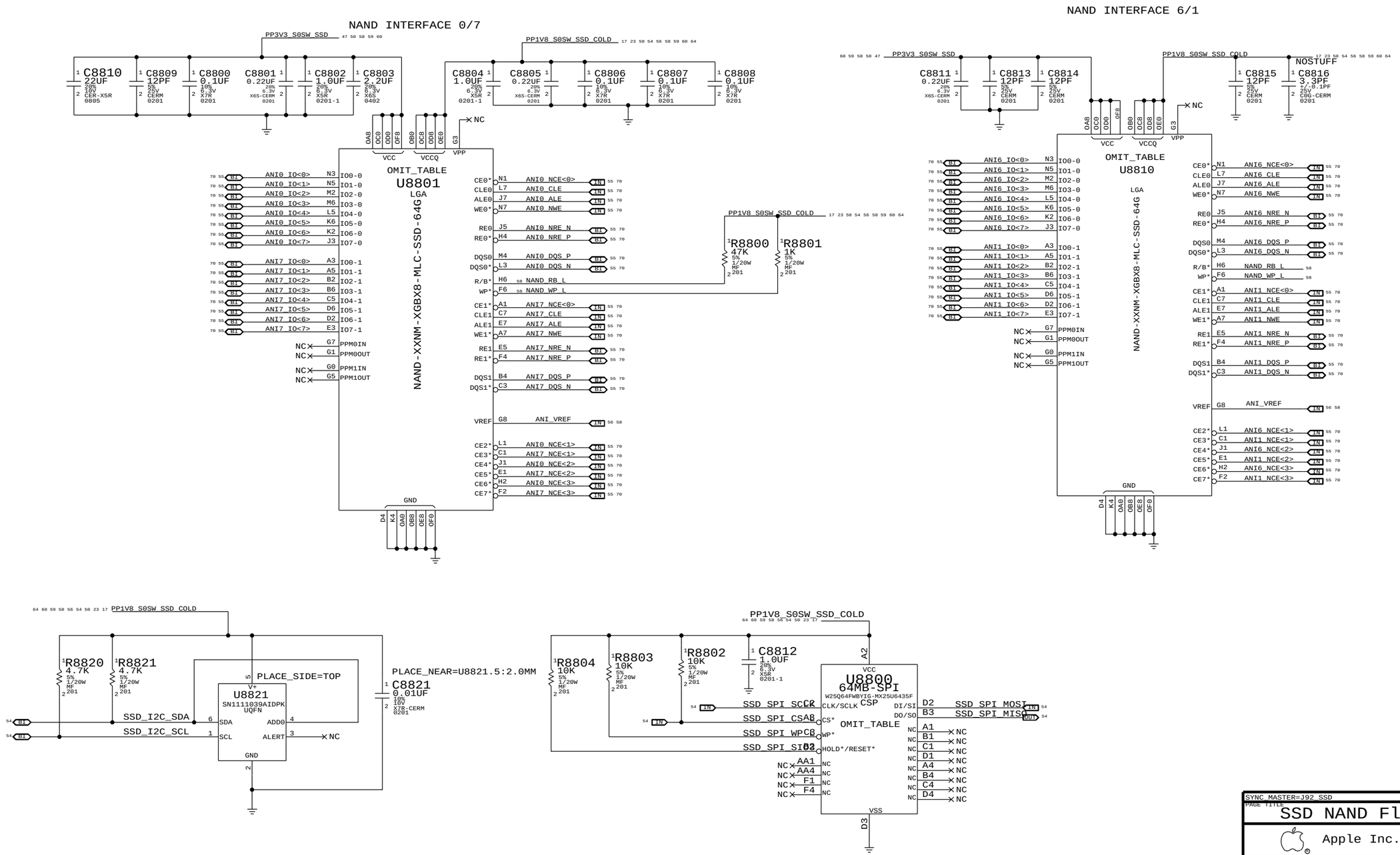

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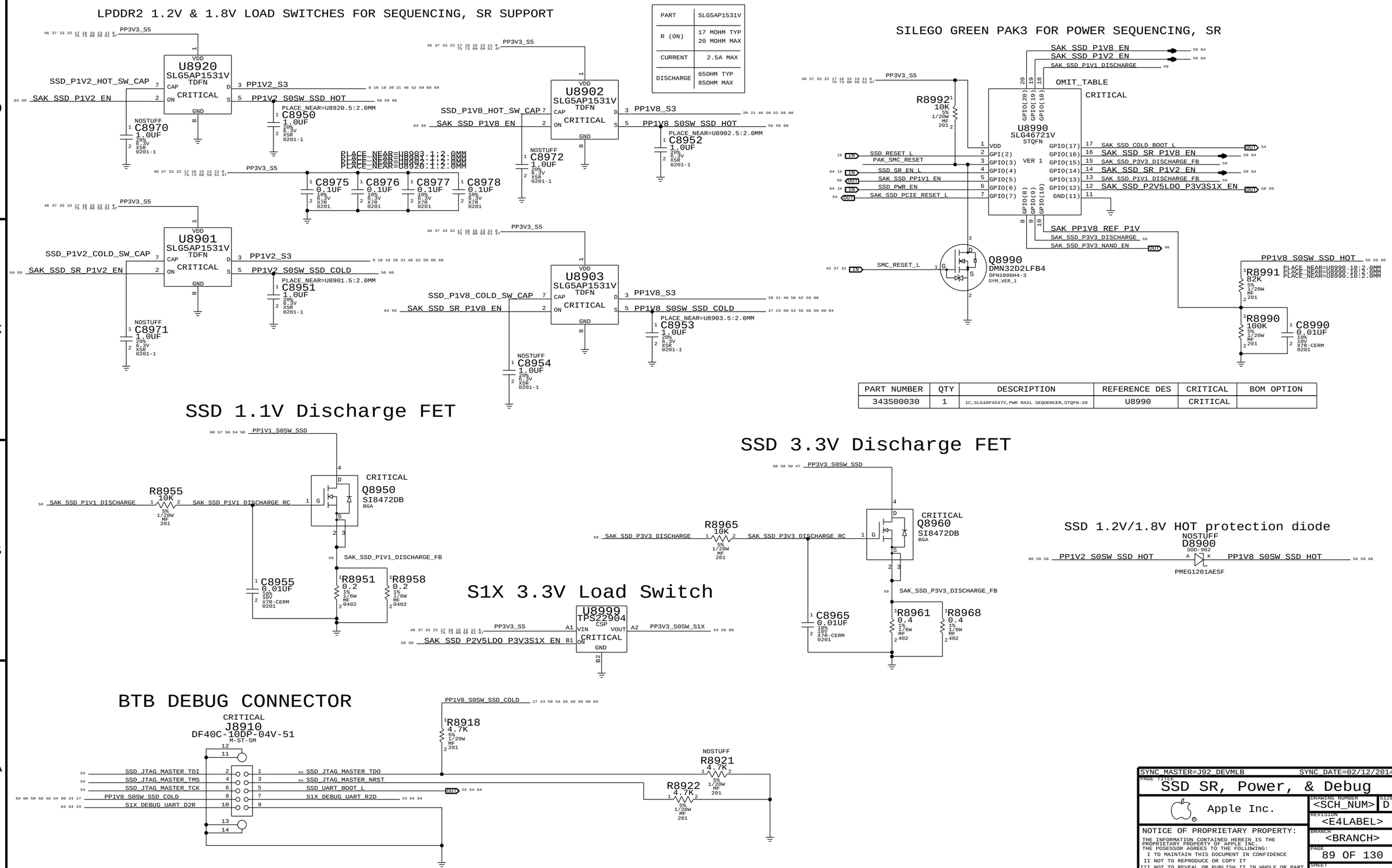

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"G3Hot" (Always-Present) Rails

PPBUS_G3H
- PPBUS_G3H — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=8.0V, MAKE_BASE=TRUE
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H
- PPBUS_G3H

PPVIN_G3H_P3V3G3H — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=8.0V, MAKE_BASE=TRUE

PPBUS_S5_HS_COMPUTING_ISNS — MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=8.0V, MAKE_BASE=TRUE
- PPBUS_S5_HS_COMPUTING_ISNS
- PPBUS_S5_HS_COMPUTING_ISNS
- PPBUS_S5_HS_COMPUTING_ISNS

PPVBUS_E85 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=20V, MAKE_BASE=TRUE
- PPVBUS_E85

PPDCIN_G3H — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=20V, MAKE_BASE=TRUE
- PPDCIN_G3H
- PPDCIN_G3H
- PPDCIN_G3H

PP3V3_G3H — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=3.42V, MAKE_BASE=TRUE
- PP3V3_G3H
- PP3V3_G3H
- PP3V3_G3H
- PP3V3_G3H
- PP3V3_G3H
- PP3V3_G3H
- PP3V3_G3H
- PP3V3_G3H

PP3V3R3V0_AON — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.1 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3R3V0_AON
- PP3V3R3V0_AON
- PP3V3R3V0_AON
- PP3V3R3V0_AON
- PP3V3R3V0_AON
- PP3V3R3V0_AON
- PP3V3R3V0_AON

PPVRTC_G3H — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.2 MM, VOLTAGE=3V, MAKE_BASE=TRUE
- PPVRTC_G3H

5V Rails

PP5V_G3H_LDO — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.1 mm, VOLTAGE=5V, MAKE_BASE=TRUE

PP5V_S0SW_LCD — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=5V, MAKE_BASE=TRUE

PP5V_S4 — MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=5V, MAKE_BASE=TRUE
- PP5V_S4
- PP5V_S4
- PP5V_S4

PP5V_S0 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.175 MM, VOLTAGE=5V, MAKE_BASE=TRUE
- PP5V_S0
- PP5V_S0
- PP5V_S0
- PP5V_S0
- PP5V_S0
- PP5V_S0
- PP5V_S0
- PP5V_S0
- PP5V_S0
- PP5V_S0

3.3V Rails

PP3V3_S5 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.15 MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5
- PP3V3_S5

PP3V3_SUS — MIN_LINE_WIDTH=0.50MM, MIN_NECK_WIDTH=0.20MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS
- PP3V3_SUS

PP3V3_S4 — MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_S4
- PP3V3_S4
- PP3V3_S4
- PP3V3_S4
- PP3V3_S4
- PP3V3_S4
- PP3V3_S4
- PP3V3_S4

PP3V3_S0 — MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=3.3V, MAKE_BASE=TRUE
- PP3V3_S0
- PP3V3_S0
- PP3V3_S0

Memory Bit/Byte Swizzle

LPDDR3 Command/Address

MAKE_BASE

=MEM_A_A<5>	TRUE	MEM_A_CAA<0>	
=MEM_A_A<9>	TRUE	MEM_A_CAA<1>	
=MEM_A_A<6>	TRUE	MEM_A_CAA<2>	
=MEM_A_A<8>	TRUE	MEM_A_CAA<3>	
=MEM_A_A<7>	TRUE	MEM_A_CAA<4>	
=MEM_A_BA<2>	TRUE	MEM_A_CAA<5>	
MEM_A_CAA<6>	TRUE	MEM_A_CAA<6>	
=MEM_A_A<11>	TRUE	MEM_A_CAA<7>	
=MEM_A_A<15>	TRUE	MEM_A_CAA<8>	
=MEM_A_A<14>	TRUE	MEM_A_CAA<9>	
=MEM_A_A<13>	TRUE	MEM_A_CAB<0>	
=MEM_A_CAS_L	TRUE	MEM_A_CAB<1>	
=MEM_A_WE_L	TRUE	MEM_A_CAB<2>	
=MEM_A_RAS_L	TRUE	MEM_A_CAB<3>	
=MEM_A_BA<0>	TRUE	MEM_A_CAB<4>	
=MEM_A_A<2>	TRUE	MEM_A_CAB<5>	
MEM_A_CAB<6>	TRUE	MEM_A_CAB<6>	
=MEM_A_A<10>	TRUE	MEM_A_CAB<7>	
=MEM_A_A<1>	TRUE	MEM_A_CAB<8>	
=MEM_A_A<0>	TRUE	MEM_A_CAB<9>	
MEM_A_ODT<0>	TRUE	MEM_A_ODT<0>	
TP_LPDDR3_RSVD1	TRUE	TP_LPDDR3_RSVD1	
TP_LPDDR3_RSVD2	TRUE	TP_LPDDR3_RSVD2	
=MEM_B_A<5>	TRUE	MEM_B_CAA<0>	
=MEM_B_A<9>	TRUE	MEM_B_CAA<1>	
=MEM_B_A<6>	TRUE	MEM_B_CAA<2>	
=MEM_B_A<8>	TRUE	MEM_B_CAA<3>	
=MEM_B_A<7>	TRUE	MEM_B_CAA<4>	
=MEM_B_BA<2>	TRUE	MEM_B_CAA<5>	
MEM_B_CAA<6>	TRUE	MEM_B_CAA<6>	
=MEM_B_A<11>	TRUE	MEM_B_CAA<7>	
=MEM_B_A<15>	TRUE	MEM_B_CAA<8>	
=MEM_B_A<14>	TRUE	MEM_B_CAA<9>	
=MEM_B_A<13>	TRUE	MEM_B_CAB<0>	
=MEM_B_CAS_L	TRUE	MEM_B_CAB<1>	
=MEM_B_WE_L	TRUE	MEM_B_CAB<2>	
=MEM_B_RAS_L	TRUE	MEM_B_CAB<3>	
=MEM_B_BA<0>	TRUE	MEM_B_CAB<4>	
=MEM_B_A<2>	TRUE	MEM_B_CAB<5>	
MEM_B_CAB<6>	TRUE	MEM_B_CAB<6>	
=MEM_B_A<10>	TRUE	MEM_B_CAB<7>	
=MEM_B_A<1>	TRUE	MEM_B_CAB<8>	
=MEM_B_A<0>	TRUE	MEM_B_CAB<9>	
MEM_B_ODT<0>	TRUE	MEM_B_ODT<0>	
TP_LPDDR3_RSVD3	TRUE	TP_LPDDR3_RSVD3	
TP_LPDDR3_RSVD4	TRUE	TP_LPDDR3_RSVD4	

MAKE_BASE

=MEM_A_DQ<0>	TRUE	MEM_A_DQ<34>	
=MEM_A_DQ<1>	TRUE	MEM_A_DQ<38>	
MEM_A_DQ<33>	TRUE	MEM_A_DQ<33>	
=MEM_A_DQ<3>	TRUE	MEM_A_DQ<36>	
=MEM_A_DQ<4>	TRUE	MEM_A_DQ<35>	
=MEM_A_DQ<5>	TRUE	MEM_A_DQ<37>	
=MEM_A_DQ<6>	TRUE	MEM_A_DQ<32>	
=MEM_A_DQ<7>	TRUE	MEM_A_DQ<39>	
=MEM_A_DQ<8>	TRUE	MEM_A_DQ<44>	
=MEM_A_DQ<9>	TRUE	MEM_A_DQ<43>	
=MEM_A_DQ<10>	TRUE	MEM_A_DQ<46>	
=MEM_A_DQ<11>	TRUE	MEM_A_DQ<45>	
=MEM_A_DQ<12>	TRUE	MEM_A_DQ<42>	
=MEM_A_DQ<13>	TRUE	MEM_A_DQ<40>	
=MEM_A_DQ<14>	TRUE	MEM_A_DQ<47>	
=MEM_A_DQ<15>	TRUE	MEM_A_DQ<41>	
=MEM_A_DQ<16>	TRUE	MEM_A_DQ<55>	
=MEM_A_DQ<17>	TRUE	MEM_A_DQ<48>	
=MEM_A_DQ<18>	TRUE	MEM_A_DQ<54>	
=MEM_A_DQ<19>	TRUE	MEM_A_DQ<53>	
=MEM_A_DQ<20>	TRUE	MEM_A_DQ<49>	
=MEM_A_DQ<21>	TRUE	MEM_A_DQ<51>	
=MEM_A_DQ<22>	TRUE	MEM_A_DQ<50>	
=MEM_A_DQ<23>	TRUE	MEM_A_DQ<52>	
=MEM_A_DQ<24>	TRUE	MEM_A_DQ<61>	
=MEM_A_DQ<25>	TRUE	MEM_A_DQ<60>	
=MEM_A_DQ<26>	TRUE	MEM_A_DQ<63>	
=MEM_A_DQ<27>	TRUE	MEM_A_DQ<62>	
=MEM_A_DQ<28>	TRUE	MEM_A_DQ<57>	
=MEM_A_DQ<29>	TRUE	MEM_A_DQ<58>	
=MEM_A_DQ<30>	TRUE	MEM_A_DQ<56>	
=MEM_A_DQ<31>	TRUE	MEM_A_DQ<59>	
=MEM_A_DQ<32>	TRUE	MEM_A_DQ<2>	
=MEM_A_DQ<33>	TRUE	MEM_A_DQ<5>	
=MEM_A_DQ<34>	TRUE	MEM_A_DQ<7>	
=MEM_A_DQ<35>	TRUE	MEM_A_DQ<3>	
=MEM_A_DQ<36>	TRUE	MEM_A_DQ<6>	
=MEM_A_DQ<37>	TRUE	MEM_A_DQ<0>	
=MEM_A_DQ<38>	TRUE	MEM_A_DQ<1>	
=MEM_A_DQ<39>	TRUE	MEM_A_DQ<4>	
=MEM_A_DQ<40>	TRUE	MEM_A_DQ<14>	
=MEM_A_DQ<41>	TRUE	MEM_A_DQ<15>	
=MEM_A_DQ<42>	TRUE	MEM_A_DQ<8>	
=MEM_A_DQ<43>	TRUE	MEM_A_DQ<11>	
=MEM_A_DQ<44>	TRUE	MEM_A_DQ<10>	
=MEM_A_DQ<45>	TRUE	MEM_A_DQ<12>	
=MEM_A_DQ<46>	TRUE	MEM_A_DQ<13>	
=MEM_A_DQ<47>	TRUE	MEM_A_DQ<9>	
=MEM_A_DQ<48>	TRUE	MEM_A_DQ<22>	
=MEM_A_DQ<49>	TRUE	MEM_A_DQ<23>	
=MEM_A_DQ<50>	TRUE	MEM_A_DQ<19>	
=MEM_A_DQ<51>	TRUE	MEM_A_DQ<17>	
=MEM_A_DQ<52>	TRUE	MEM_A_DQ<21>	
=MEM_A_DQ<53>	TRUE	MEM_A_DQ<16>	
=MEM_A_DQ<54>	TRUE	MEM_A_DQ<18>	
=MEM_A_DQ<55>	TRUE	MEM_A_DQ<20>	
=MEM_A_DQ<56>	TRUE	MEM_A_DQ<24>	
=MEM_A_DQ<57>	TRUE	MEM_A_DQ<29>	
=MEM_A_DQ<58>	TRUE	MEM_A_DQ<26>	
=MEM_A_DQ<59>	TRUE	MEM_A_DQ<28>	
=MEM_A_DQ<60>	TRUE	MEM_A_DQ<25>	
=MEM_A_DQ<61>	TRUE	MEM_A_DQ<31>	
=MEM_A_DQ<62>	TRUE	MEM_A_DQ<30>	
=MEM_A_DQ<63>	TRUE	MEM_A_DQ<27>	
=MEM_A_DQS_P<0>	TRUE	MEM_A_DQS_P<4>	
=MEM_A_DQS_N<0>	TRUE	MEM_A_DQS_N<4>	
=MEM_A_DQS_P<1>	TRUE	MEM_A_DQS_P<5>	
=MEM_A_DQS_N<1>	TRUE	MEM_A_DQS_N<5>	
MEM_A_DQS_P<6>	TRUE	MEM_A_DQS_P<6>	
MEM_A_DQS_N<6>	TRUE	MEM_A_DQS_N<6>	
=MEM_A_DQS_P<3>	TRUE	MEM_A_DQS_P<7>	
=MEM_A_DQS_N<3>	TRUE	MEM_A_DQS_N<7>	
=MEM_A_DQS_P<4>	TRUE	MEM_A_DQS_P<0>	
=MEM_A_DQS_N<4>	TRUE	MEM_A_DQS_N<0>	
=MEM_A_DQS_P<5>	TRUE	MEM_A_DQS_P<1>	
=MEM_A_DQS_N<5>	TRUE	MEM_A_DQS_N<1>	
=MEM_A_DQS_P<6>	TRUE	MEM_A_DQS_P<2>	
=MEM_A_DQS_N<6>	TRUE	MEM_A_DQS_N<2>	
=MEM_A_DQS_P<7>	TRUE	MEM_A_DQS_P<3>	
=MEM_A_DQS_N<7>	TRUE	MEM_A_DQS_N<3>	

MAKE_BASE

=MEM_B_DQ<0>	TRUE	MEM_B_DQ<35>	
=MEM_B_DQ<1>	TRUE	MEM_B_DQ<38>	
MEM_B_DQ<32>	TRUE	MEM_B_DQ<32>	
=MEM_B_DQ<3>	TRUE	MEM_B_DQ<36>	
=MEM_B_DQ<4>	TRUE	MEM_B_DQ<37>	
=MEM_B_DQ<5>	TRUE	MEM_B_DQ<39>	
=MEM_B_DQ<6>	TRUE	MEM_B_DQ<34>	
=MEM_B_DQ<7>	TRUE	MEM_B_DQ<33>	
=MEM_B_DQ<8>	TRUE	MEM_B_DQ<41>	
=MEM_B_DQ<9>	TRUE	MEM_B_DQ<43>	
=MEM_B_DQ<10>	TRUE	MEM_B_DQ<46>	
=MEM_B_DQ<11>	TRUE	MEM_B_DQ<45>	
=MEM_B_DQ<12>	TRUE	MEM_B_DQ<47>	
=MEM_B_DQ<13>	TRUE	MEM_B_DQ<44>	
=MEM_B_DQ<14>	TRUE	MEM_B_DQ<42>	
=MEM_B_DQ<15>	TRUE	MEM_B_DQ<40>	
=MEM_B_DQ<16>	TRUE	MEM_B_DQ<55>	
=MEM_B_DQ<17>	TRUE	MEM_B_DQ<50>	
=MEM_B_DQ<18>	TRUE	MEM_B_DQ<48>	
=MEM_B_DQ<19>	TRUE	MEM_B_DQ<53>	
=MEM_B_DQ<20>	TRUE	MEM_B_DQ<51>	
=MEM_B_DQ<21>	TRUE	MEM_B_DQ<52>	
=MEM_B_DQ<22>	TRUE	MEM_B_DQ<54>	
=MEM_B_DQ<23>	TRUE	MEM_B_DQ<49>	
=MEM_B_DQ<24>	TRUE	MEM_B_DQ<60>	
=MEM_B_DQ<25>	TRUE	MEM_B_DQ<57>	
=MEM_B_DQ<26>	TRUE	MEM_B_DQ<59>	
=MEM_B_DQ<27>	TRUE	MEM_B_DQ<63>	
=MEM_B_DQ<28>	TRUE	MEM_B_DQ<61>	
=MEM_B_DQ<29>	TRUE	MEM_B_DQ<56>	
=MEM_B_DQ<30>	TRUE	MEM_B_DQ<58>	
=MEM_B_DQ<31>	TRUE	MEM_B_DQ<62>	
=MEM_B_DQ<32>	TRUE	MEM_B_DQ<6>	
=MEM_B_DQ<33>	TRUE	MEM_B_DQ<0>	
=MEM_B_DQ<34>	TRUE	MEM_B_DQ<3>	
=MEM_B_DQ<35>	TRUE	MEM_B_DQ<5>	
=MEM_B_DQ<36>	TRUE	MEM_B_DQ<7>	
=MEM_B_DQ<37>	TRUE	MEM_B_DQ<1>	
=MEM_B_DQ<38>	TRUE	MEM_B_DQ<4>	
=MEM_B_DQ<39>	TRUE	MEM_B_DQ<2>	
=MEM_B_DQ<40>	TRUE	MEM_B_DQ<8>	
=MEM_B_DQ<41>	TRUE	MEM_B_DQ<11>	
=MEM_B_DQ<42>	TRUE	MEM_B_DQ<9>	
=MEM_B_DQ<43>	TRUE	MEM_B_DQ<12>	
=MEM_B_DQ<44>	TRUE	MEM_B_DQ<15>	
=MEM_B_DQ<45>	TRUE	MEM_B_DQ<14>	
=MEM_B_DQ<46>	TRUE	MEM_B_DQ<13>	
=MEM_B_DQ<47>	TRUE	MEM_B_DQ<10>	
=MEM_B_DQ<48>	TRUE	MEM_B_DQ<23>	
=MEM_B_DQ<49>	TRUE	MEM_B_DQ<18>	
=MEM_B_DQ<50>	TRUE	MEM_B_DQ<19>	
=MEM_B_DQ<51>	TRUE	MEM_B_DQ<17>	
=MEM_B_DQ<52>	TRUE	MEM_B_DQ<20>	
=MEM_B_DQ<53>	TRUE	MEM_B_DQ<16>	
=MEM_B_DQ<54>	TRUE	MEM_B_DQ<22>	
=MEM_B_DQ<55>	TRUE	MEM_B_DQ<21>	
=MEM_B_DQ<56>	TRUE	MEM_B_DQ<29>	
=MEM_B_DQ<57>	TRUE	MEM_B_DQ<25>	
=MEM_B_DQ<58>	TRUE	MEM_B_DQ<24>	
=MEM_B_DQ<59>	TRUE	MEM_B_DQ<26>	
=MEM_B_DQ<60>	TRUE	MEM_B_DQ<27>	
=MEM_B_DQ<61>	TRUE	MEM_B_DQ<28>	
=MEM_B_DQ<62>	TRUE	MEM_B_DQ<30>	
=MEM_B_DQ<63>	TRUE	MEM_B_DQ<31>	
=MEM_B_DQS_P<0>	TRUE	MEM_B_DQS_P<4>	
=MEM_B_DQS_N<0>	TRUE	MEM_B_DQS_N<4>	
=MEM_B_DQS_P<1>	TRUE	MEM_B_DQS_P<5>	
=MEM_B_DQS_N<1>	TRUE	MEM_B_DQS_N<5>	
MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<6>	
MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<6>	
=MEM_B_DQS_P<3>	TRUE	MEM_B_DQS_P<7>	
=MEM_B_DQS_N<3>	TRUE	MEM_B_DQS_N<7>	
=MEM_B_DQS_P<4>	TRUE	MEM_B_DQS_P<0>	
=MEM_B_DQS_N<4>	TRUE	MEM_B_DQS_N<0>	
=MEM_B_DQS_P<5>	TRUE	MEM_B_DQS_P<1>	
=MEM_B_DQS_N<5>	TRUE	MEM_B_DQS_N<1>	
=MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<2>	
=MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<2>	
=MEM_B_DQS_P<7>	TRUE	MEM_B_DQS_P<3>	
=MEM_B_DQS_N<7>	TRUE	MEM_B_DQS_N<3>	

TP_CPU_MEMVTT_PWR_EN_LSVDDQ — TP_CPU_MEMVTT_PWR_EN_LSVDDQ
MAKE_BASE=TRUE

SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
PAGE TITLE: Memory Signal Swaps	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
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		MAKE_BASE		
64 62 28 15	QR SWITCH EN		QR SWITCH EN	15 28 62 64
62 44 8	CPU VR READY	TRUE	CPU VR READY	8 44 62
62 31 13	SMC PCH SUSWARN L	TRUE	SMC PCH SUSWARN L	13 31 62
62 31 13	SMC PCH SUSACK L	TRUE	SMC PCH SUSACK L	13 31 62
62 43 35 32 31	SMC BC ACOK	TRUE	SMC BC ACOK	31 32 35 43 62
62 5	TP ULX SPARE1	TRUE	TP ULX SPARE1	5 62
62 5	TP ULX SSP SPARE	TRUE	TP ULX SSP SPARE	5 62
68 62 12	TP LPC CLK24M LPCPLUS R	TRUE	TP LPC CLK24M LPCPLUS R	12 62 68
64 62 28 13	HPM I2C INT L	TRUE	HPM I2C INT L	13 28 62 64
64 62 28 13	HPM I2C INT L			
63 62 28 16 14 64	XDP USB EXTA OC L	TRUE	XDP USB EXTA OC L	14 16 28 62 63 64
62 37 32 31 26	SMC TCK	TRUE	SMC TCK	26 31 32 37 62
62 37 32 31 26	SMC TMS	TRUE	SMC TMS	26 31 32 37 62
62 28	TP HPM XTALOUT	TRUE	TP HPM XTALOUT	28 62
	GND	TRUE	GND	
68 64 62 29 12	PCIE CLK100M TBT P	TRUE	PCIE CLK100M TBT P	12 29 62 64 68
68 64 62 29 12	PCIE CLK100M TBT N	TRUE	PCIE CLK100M TBT N	12 29 62 64 68
29	=PCIE E85 D2R P	TRUE	PCIE TBT D2R P<0>	14 68
29	=PCIE E85 D2R N	TRUE	PCIE TBT D2R N<0>	14 68
29	=PCIE E85 R2D P	TRUE	PCIE TBT R2D C P<0>	14 68
29	=PCIE E85 R2D N	TRUE	PCIE TBT R2D C N<0>	14 68
62 29 12	TBT CLKREQ L	TRUE	TBT CLKREQ L	12 29 62
62 29 15	PCH TBT PCIE RESET L	TRUE	PCH TBT PCIE RESET L	15 29 62
64 62 29 28	E85 TEST MODE L	TRUE	E85 TEST MODE L	28 29 62 64

64 62 50 29 28 27 IN E85HSMUX_USB_EN — E85HSMUX_USB_EN OUT 27 28 29 50 62 64
MAKE_BASE=TRUE

SYNC_MASTER=J92_DEVMLB SYNC_DATE=07/08/2014

PAGE TITLE
J92 Signal Aliases

Apple Inc.

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REVISION <E4LABEL>

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NO_TEST Nets

		NO_TEST	MAKE_BASE			
63 12	NC_PCIE_CLK100M_SDP	TRUE	TRUE	NC_PCIE_CLK100M_SDP	12 63	CPU/PCH
63 12	NC_PCIE_CLK100M_SDN	TRUE	TRUE	NC_PCIE_CLK100M_SDN	12 63	
63	NC_PCIE_TBT_D2RP<1>	TRUE	TRUE	NC_PCIE_TBT_D2RP<1>	63	
63	NC_PCIE_TBT_D2RN<1>	TRUE	TRUE	NC_PCIE_TBT_D2RN<1>	63	
63	NC_PCIE_TBT_R2D_CP<1>	TRUE	TRUE	NC_PCIE_TBT_R2D_CP<1>	63	
63	NC_PCIE_TBT_R2D_CN<1>	TRUE	TRUE	NC_PCIE_TBT_R2D_CN<1>	63	
63 14	NC_USB_CAMERAP	TRUE	TRUE	NC_USB_CAMERAP	14 63	
63 14	NC_USB_CAMERAN	TRUE	TRUE	NC_USB_CAMERAN	14 63	
63 14	NC_USB_SDP	TRUE	TRUE	NC_USB_SDP	14 63	
63 14	NC_USB_SDN	TRUE	TRUE	NC_USB_SDN	14 63	
63 12	NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1	12 63	
63 13	NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L	13 63	
63 14	NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK	14 63	
63 14	NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA	14 63	
63 14	NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L	14 63	
	=DP_TBTSNK1_ML_C_P<3..0>	TRUE	TRUE	NC_DP_TBTSNK1_ML_CP<3..0>	5	
	=DP_TBTSNK1_ML_C_N<3..0>	TRUE	TRUE	NC_DP_TBTSNK1_ML_CN<3..0>	5	
63 13	NC_DP_TBTSNK1_DDC_CLK	TRUE	TRUE	NC_DP_TBTSNK1_DDC_CLK	13 63	
63 13	NC_DP_TBTSNK1_DDC_DATA	TRUE	TRUE	NC_DP_TBTSNK1_DDC_DATA	13 63	
63 13	NC_DP_TBTSNK1_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSNK1_AUXCH_CP	13 63	
63 13	NC_DP_TBTSNK1_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSNK1_AUXCH_CN	13 63	
63 13	NC_DP_TBTSNK1_HPD	TRUE	TRUE	NC_DP_TBTSNK1_HPD	13 63	
63 31	NC_SMC_SYS_LED	TRUE	TRUE	NC_SMC_SYS_LED	31 63	SMC
63	NC_SMC_DEBUGPRT_EN_L	TRUE	TRUE	NC_SMC_DEBUGPRT_EN_L	63	
63 31	NC_SMC_SYS_KBDLED	TRUE	TRUE	NC_SMC_SYS_KBDLED	31 63	
63	NC_SMC_T25_EN_L	TRUE	TRUE	NC_SMC_T25_EN_L	63	
63 31	NC_SMC_GFX_THROTTLE_L	TRUE	TRUE	NC_SMC_GFX_THROTTLE_L	31 63	
63 31	NC_SMC_FAN_0_TACH	TRUE	TRUE	NC_SMC_FAN_0_TACH	31 63	
63 31	NC_SMC_FAN_1_CTL	TRUE	TRUE	NC_SMC_FAN_1_CTL	31 63	
63 31	NC_SMC_FAN_1_TACH	TRUE	TRUE	NC_SMC_FAN_1_TACH	31 63	
63 31	NC_SMBUS_SMC_4_ASF_SCL	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SCL	31 63	
63 31	NC_SMBUS_SMC_4_ASF_SDA	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SDA	31 63	
64 63 31	NC_SYS_ONEWIRE	TRUE	TRUE	NC_SYS_ONEWIRE	31 63 64	

Unused nets with offpage

(Nets with offpages not used on this project)

SD_RESET_L	15
SD_PWR_EN	15
ENET_MEDIA_SENSE	15
BT_PWRRST_L	15
TPAD_USB_IF_EN	15
PCH_GPIO12	15
TBT_PWR_EN	15
TBT_CIO_PLUG_EVENT_L	15
JTAG_TBT_TMS_PCH	15
ODD_PWR_EN_L	13
HDMITBTMUX_FLAG	13
HDMITBTMUX_LATCH	13
CAM_SENSOR_WAKE_L	24
LCD_PSR_EN	15
XDP_USB_EXTA_OC_L	14 16 28 62 64
AUD_WAKE_L	15
MIKEY_SPI_CS_L	15
MIKEY_SPI_CLK	15
MIKEY_SPI_MISO	15
MIKEY_SPI_MOSI	15

SYNC_MASTER=J92_DEVMLB SYNC_DATE=07/08/2014

PAGE TITLE
Func Test / No Test

Apple Inc.

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EE Chaz Probe Points

PPA501	P3V3S3_EN	MAKE_BASE=TRUE	P3V3S3_EN	46 64
PPA502	PMIC2_READY			46 48
PPA503	P1V05SUS_DRVH			48
PPA504	SMC_CBC_ON			31 43
PPA505	SMC_CHGR_INT_L			31 43
PPA506	MEM_B_CAA<0>			21 61 69
PPA507	MEM_B_CLK_P<0>			7 21 69
PPA508	MEM_B_CLK_N<0>			7 21 69
PPA509	MEM_B_CS_L<0>			7 21 69
PPA510	MEM_B_DQ<0>			7 61 69
PPA511	MEM_B_DQS_P<0>			7 61 69
PPA512	MEM_B_DQS_N<0>			7 61 69
PPA513	AP_PCIE_DEV_WAKE			13 22
PPA514	AP_S0IX_WAKE_L			15 22
PPA515	AP_S0IX_WAKE_SEL			15 22
PPA516	E85HSMUX_USB_EN			27 28 29 50 62
PPA519	PCH_BT_UART_D2R			15 23
PPA520	BT_UART_CTS_L			22 23
PPA521	PCH_UART1_R2D			15
PPA522	PCIE_CAMERA_D2R_P			14 25 68
PPA523	PCIE_CLK100M_SSD_P			12 54 64 66
PPA524	PCIE_CLK100M_TBT_P			12 29 62 68
	AGND_PMIC	MAKE_BASE=TRUE	AGND_PMIC	46 48 64
	AGND_PMIC			64 48 46
	AGND_PMIC			64 48 46
	AGND_PMIC			64 48 46
	AGND_PMIC			64 48 46
	TS_HIPWR_EN	MAKE_BASE=TRUE	TS_HIPWR_EN	28 31 43 64
	TS_POWER_GATE_EN	MAKE_BASE=TRUE	TS_POWER_GATE_EN	28 43 64
	SSD_PWR_EN	MAKE_BASE=TRUE	SSD_PWR_EN	15 59 64
	SSD_UART_BOOT_L	MAKE_BASE=TRUE	SSD_UART_BOOT_L	23 54 59 64
	S1X_DEBUG_UART_D2R	MAKE_BASE=TRUE	S1X_DEBUG_UART_D2R	23 54 59 64
	S1X_DEBUG_UART_R2D	MAKE_BASE=TRUE	S1X_DEBUG_UART_R2D	23 54 59 64
	PP1V8_S0SW_SSD_COLD	MAKE_BASE=TRUE	PP1V8_S0SW_SSD_COLD	64 56 58 17 23 59 62 59 60
	PCIE_CLK100M_SSD_P	MAKE_BASE=TRUE	PCIE_CLK100M_SSD_P	12 54 64 66
	PCIE_CLK100M_SSD_N	MAKE_BASE=TRUE	PCIE_CLK100M_SSD_N	12 54 64 66
	=PCIE_SSD_D2R_P<0..3>	MAKE_BASE=TRUE	PCIE_SSD_D2R_P<0..3>	14 64 66
	=PCIE_SSD_D2R_N<0..3>	MAKE_BASE=TRUE	PCIE_SSD_D2R_N<0..3>	14 64 66
	=PCIE_SSD_R2D_P<0..3>	MAKE_BASE=TRUE	PCIE_SSD_R2D_P<0..3>	23 66
	=PCIE_SSD_R2D_N<0..3>	MAKE_BASE=TRUE	PCIE_SSD_R2D_N<0..3>	23 66
	P1V1_S0_DLPN_PGOOD	MAKE_BASE=TRUE	P1V1_S0_DLPN_PGOOD	46 64
	SYSCLK_CLK24M_CAMERA	MAKE_BASE=TRUE	SYSCLK_CLK24M_CAMERA	17 24 64 68
	SYSCLK_CLK32K_PMIC	MAKE_BASE=TRUE	SYSCLK_CLK32K_PMIC	17 46 64
	TP_SMC_PWRFAIL_WARN_L	MAKE_BASE=TRUE	TP_SMC_PWRFAIL_WARN_L	31 64

PPA525	E85_RFU<1>	26 29
PPA526	E85_RFU<2>	26 29
PPA527	E85_CC1	29 60 68
PPA528	E85_CC2	29 60 68
PPA529	AUD_PWR_EN	13 40
PPA530	BT_UART_RTS_L	22 23
PPA531	CAMERA_PWR_EN	15 24
PPA532	HPM_I2C_INT_L	13 28 62
PPA533	EDP_BKLT_PWM	13 53
PPA534	HDA_SDIN0	12 40 68
PPA535	I2C_PCH_1_SCL	15 28 34
PPA536	I2C_PCH_1_SDA	15 28 34
PPA537	LCD_IRQ_L	15 53
PPA538	MEM_CAM_A<8>	24 25 71
PPA539	MEM_CAM_CS_L	24 25 71
PPA545	PCH_BT_UART_CTS_L	15 23
PPA546	PCH_BT_UART_R2D	15 23
PPA547	PCH_UART1_D2R	15
PPA548	PCIE_CAMERA_D2R_N	14 25 68
PPA549	PCIE_CLK100M_SSD_N	12 54 64 66
PPA550	PCIE_CLK100M_TBT_N	12 29 62 68
PPA551	PCIE_SSD_D2R_N<0>	14 64 66
PPA552	PCIE_SSD_D2R_P<0>	14 64 66
PPA555	QR_SWITCH_EN	15 28 62
PPA556	SAK_SSD_P1V2_EN	59
PPA557	SAK_SSD_P1V8_EN	59
PPA558	SAK_SSD_SR_P1V2_EN	59
PPA559	SAK_SSD_SR_P1V8_EN	59
PPA560	SMC_BT_PWR_EN	22 31
PPA561	SMC_CLK32K_PMIC	31 32
PPA562	SMC_OOB1_R2D_L	31 54
PPA563	SMC_PROCHOT	31 32
PPA564	SMC_SENSOR_PWR_EN	31 33 35
PPA565	SMC_WAKE_SCI_L	15 31
PPA566	SMC_WIFI_PWR_EN	22 31
PPA567	AP_PCIE_WAKE_L	22
PPA568	SSD_BOOT	13 23
PPA569	SSD_SR_EN_L	15 59
PPA570	SYSCLK_CLK12M_SMC	17 31
PPA571	SYSCLK_CLK12M_SSD	17 54
PPA572	SYSCLK_CLK24M_CAMERA	17 24 64 68
PPA573	SYSCLK_CLK32K_PMIC	17 46 64
PPA574	BT_DEV_WAKE	22
PPA575	TPAD_SPI_CS_L	15 30
PPA576	TPAD_SPI_INT_L	15 30

PPA577	USB3_EXTA_D2R_N	14 29 67
PPA578	USB3_EXTA_D2R_P	14 29 67
PPA579	CPU_CATERR_L	6 31 66
PPA580	E85_TEST_MODE_L	28 29 62
PPA581	MEM_B_CS_L<1>	7 21 69
PPA582	MEM_B_CKE<1>	7 21 69
PPA583	MEM_B_CAB<1>	21 61 69
PPA584	MEM_B_CAA<2>	21 61 69
PPA585	MCP_RSVD_CK13 (MAKE_BASE=TRUE)	MCP_RSVD_CK13 — 6 64
PPA586	MCP_DC_CV45 (MAKE_BASE=TRUE)	MCP_DC_CV45 — 8 64
PPA587	MEM_B_CAA<3>	21 61 69
PPA588	E85_LS_P<1>	26 29 68
PPA589	E85_LS_N<1>	26 29 68
PPA590	E85_LS_P<2>	26 29 68
PPA591	E85_LS_N<2>	26 29 68
PPA592	XDP_PCH_UART_SSD_L_BT_H	12 16
PPA593	DP_E85SNK_HPD	18 28 33
PPA594	XDP_USB_EXTA_OC_L	14 16 28 62 63
PPA595	XDP_USB_EXTB_OC_L	14 16 64
PPA596	USB_EXTA_P	14 26 67
PPA597	USB_EXTA_N	14 26 67
PPA5A0	BBPD_IPU_EN	28 29
PPA5A1	BBPD_MISO_LS1V1	29
PPA5A2	BBPD_PD_EN	28 29
PPA5A3	BBPD_PD_SEL_CC2	28 29
PPA5A4	BBPD_RPD_EN	28 29
PPA5A5	BBPD_RX_L_TX_H	28 29
PPA5A6	BBPD_SPI_MOSI	28 29
PPA5A7	BBPD_VCONN1_EN	29 50
PPA5A8	BBPD_VCONN2_EN	29 50
PPA5A9	BBPD_VCONN_EN	28 29

64 7	TP_ULX_DDR_VCCDDQG	TRUE	TP_ULX_DDR_VCCDDQG — 7 64
67 64 32 31 26	SMC_DEBUGPRT_TX_L	TRUE	SMC_DEBUGPRT_TX_L — 26 31 32 64 67
67 64 32 31 26	SMC_DEBUGPRT_RX_L	TRUE	SMC_DEBUGPRT_RX_L — 26 31 32 64 67

NO_TEST Nets

		NO_TEST	MAKE_BASE		
67 64 14	NC_USB3_EXTB_D2RP	TRUE	TRUE	NC_USB3_EXTB_D2RP	67 64 14
67 64 14	NC_USB3_EXTB_D2RN	TRUE	TRUE	NC_USB3_EXTB_D2RN	67 64 14
67 64 14	NC_USB3_EXTB_R2D_CP	TRUE	TRUE	NC_USB3_EXTB_R2D_CP	14 64 67
67 64 14	NC_USB3_EXTB_R2D_CN	TRUE	TRUE	NC_USB3_EXTB_R2D_CN	14 64 67
64 14	NC_USB_IRP	TRUE	TRUE	NC_USB_IRP	14 64
64 14	NC_USB_IRN	TRUE	TRUE	NC_USB_IRN	14 64
67 64 14	NC_USB_EXTBP	TRUE	TRUE	NC_USB_EXTBP	67 64 14
67 64 14	NC_USB_EXTBN	TRUE	TRUE	NC_USB_EXTBN	67 64 14
67 64 14	NC_USB_TPADP	TRUE	TRUE	NC_USB_TPADP	67 64 14
67 64 14	NC_USB_TPADN	TRUE	TRUE	NC_USB_TPADN	67 64 14
64 12	NC_PCIE_CLK100M_FWP	TRUE	TRUE	NC_PCIE_CLK100M_FWP	12 64
64 12	NC_PCIE_CLK100M_FWN	TRUE	TRUE	NC_PCIE_CLK100M_FWN	12 64
64 63 31	NC_SYS_ONEWIRE	TRUE	TRUE	NC_SYS_ONEWIRE	31 63 64
64 46	NC_PMIC_CLK32K_XTALIN	TRUE	TRUE	NC_PMIC_CLK32K_XTALIN	46 64
64 31	NC_SMC_GFX_OVERTEMP	TRUE	TRUE	NC_SMC_GFX_OVERTEMP	31 64
64 31	NC_SMC_FAN_0_CTL	TRUE	TRUE	NC_SMC_FAN_0_CTL	31 64
64 31	NC_SMC_FAN_4_CTL	TRUE	TRUE	NC_SMC_FAN_4_CTL	31 64

CPU/PCH 14 64 67

Unused nets with offpage

(Nets with offpages not used on this project)

U770	XDP_USB_EXTB_OC_L	14 16 64

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PAGE TITLE: Project FCT/NC/Aliases

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J92 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,MEM_TERM	MM	16.5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL6,ISL8,ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3,ISL4	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	Y	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.260 MM			
27P4_OHM_SE	ISL6,ISL8,ISL10	Y	0.134 MM	0.134 MM			
27P4_OHM_SE	ISL3,ISL4	Y	0.190 MM	0.190 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.144 MM	0.144 MM			
40_OHM_SE	ISL6	Y	0.070 MM	0.070 MM			
40_OHM_SE	ISL8	Y	0.073 MM	0.073 MM			
40_OHM_SE	ISL10	Y	0.071 MM	0.071 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.120 MM	0.095 MM			
45_OHM_SE	ISL6	Y	0.057 MM	0.057 MM			
45_OHM_SE	ISL8	Y	0.058 MM	0.058 MM			
45_OHM_SE	ISL10	Y	0.057 MM	0.057 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE_RF	TOP,BOTTOM	Y	0.225 MM	0.225 MM			
50_OHM_SE_RF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	TOP,BOTTOM	Y	0.147 MM	0.060 MM		0.100 MM	0.100 MM
70_OHM_DIFF	ISL6	Y	0.082 MM	0.082 MM	=STANDARD	0.080 MM	0.080 MM
70_OHM_DIFF	ISL8	Y	0.085 MM	0.085 MM	=STANDARD	0.080 MM	0.080 MM
70_OHM_DIFF	ISL10	Y	0.081 MM	0.081 MM	=STANDARD	0.080 MM	0.080 MM
70_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.060 MM		0.100 MM	0.100 MM
85_OHM_DIFF	ISL6,ISL9,ISL11	Y	0.058 MM	0.058 MM	=STANDARD	0.100 MM	0.100 MM
85_OHM_DIFF	ISL8	Y	0.060 MM	0.060 MM	=STANDARD	0.100 MM	0.100 MM
85_OHM_DIFF	ISL10	Y	0.057 MM	0.057 MM	=STANDARD	0.100 MM	0.100 MM
85_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Note: 80ohm copied from 85ohm (pending stack-up calcs)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.060 MM		0.100 MM	0.100 MM
80_OHM_DIFF	ISL6,ISL9,ISL11	Y	0.058 MM	0.058 MM	=STANDARD	0.100 MM	0.100 MM
80_OHM_DIFF	ISL8	Y	0.060 MM	0.060 MM	=STANDARD	0.100 MM	0.100 MM
80_OHM_DIFF	ISL10	Y	0.056 MM	0.056 MM	=STANDARD	0.101 MM	0.101 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.057 MM	?
1x_DIELECTRIC	ISL2,ISL11	0.057 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.057 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.054 MM	?
1x_DIELECTRIC	ISL5,ISL8	0.058 MM	?
1x_DIELECTRIC	ISL6,ISL7	0.051 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	P070MM_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM

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PAGE TITLE: PCB Rule Definitions

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_4S	*	=4S_OHM_SE	=4S_OHM_SE	=4S_OHM_SE	=4S_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

Note: DisplayPort tables are on Page 113

CPU Net Properties

Note: 80ohm constraints are actually 85ohm

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CPU_PECI	CPU_4S	CPU_COMP	CPU_PECI	6 32
PM_SYNC	CPU_4S	CPU_AGTL	PM_SYNC	
PM_MEM_PWRGD	CPU_4S	CPU_AGTL	PM_MEM_PWRGD	
	CPU_4S	CPU_ITP	XDP_DBRESET_L	16 17
	CPU_4S	CPU_ITP	XDP_CPU_PRDY_L	6 16
	CPU_4S	CPU_ITP	XDP_CPU_PREQ_L	6 16
	CPU_27P4S	CPU_COMP	EDP_COMP	
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	6
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	6
CPU_CFG	CPU_4S	CPU_ITP	CPU_CFG<2..0>	6 16
CPU_CFG3	CPU_4S	CPU_ITP	CPU_CFG<3>	6 16
CPU_CFG	CPU_4S	CPU_ITP	CPU_CFG<19..4>	6 16
CPU_CATERR_L	CPU_4S	CPU_AGTL	CPU_CATERR_L	6 31 64
	CPU_4S	CPU_AGTL	CPU_VCCIO_SEL	
CPU_PROCHOT_L	CPU_4S	CPU_AGTL	CPU_PROCHOT_L	6 31 32 44
CPU_PWRGD	CPU_4S	CPU_AGTL	CPU_PWRGD	6
PM_THRMTRIP_L	CPU_4S	CPU_8MIL	PM_THRMTRIP_L	15 31 32
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P	
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	
XDP_TDI	CPU_4S	CPU_ITP	XDP_CPU_TDI	6 16
XDP_TDO	CPU_4S	CPU_ITP	XDP_CPU_TDO	6 16
XDP_TMS	CPU_4S	CPU_ITP	XDP_CPU_TMS	6 16
XDP_TCK	CPU_4S	CPU_ITP	XDP_CPU_TCK	6 16
XDP_TRST_L	CPU_4S	CPU_ITP	XDP_CPUPCH_TRST_L	6 12 16
XDP_BPM_L	CPU_4S	CPU_ITP	XDP_BPM_L<1..0>	6 16
	CPU_4S	CPU_ITP	XDP_BPM_L<7..2>	6 16
	CPU_4S	CPU_ITP	XDP_OBSDATA_B<3..0>	
(FSB_CPURST_L)	CPU_4S	CPU_ITP	XDP_CPURST_L	16
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	8 44
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	9 44
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
CPU_SVIDALERT_L	CPU_4S	CPU_COMP	CPU_VIDALERT_L	8 44
CPU_SVIDSCLK	CPU_4S	CPU_COMP	CPU_VIDSCLK	8 44
CPU_SVIDSOUT	CPU_4S	CPU_COMP	CPU_VIDSOUT	8 44
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	14 23
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	14 23
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	23 64
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	23 64
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>	54
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>	54
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0>	14 64
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0>	14 64
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 54 64
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 54 64
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_E85SNK_AUXCH_P	26 29
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_E85SNK_AUXCH_N	26 29
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	13 29
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	13 29
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	53
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	53
	DP_80D	DP_TX	DP_INT_ML_C_P<3..0>	5 53
	DP_80D	DP_TX	DP_INT_ML_C_N<3..0>	5 53
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P	5 53
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N	5 53
	DP_80D	DP_AUX	DP_INT_AUX_P	53
	DP_80D	DP_AUX	DP_INT_AUX_N	53

PCIe SSD

DP

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

E85 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
E85_HS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
E85_LS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
E85_HS	*	=6x_DIELECTRIC	?
E85_LS	*	=4x_DIELECTRIC	?
E85_CC	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
E85_HS	TOP,BOTTOM	=10x_DIELECTRIC	?
E85_LS	TOP,BOTTOM	=6x_DIELECTRIC	?
E85_CC	TOP,BOTTOM	=6x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS
USB3_PCH_TX	*	*	USB3_2OTHER
USB3_PCH_RX	*	*	USB3_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_TX2TX	*	=2.5x_DIELECTRIC	?
USB3_RX2RX	*	=2.5x_DIELECTRIC	?
USB3_TX2OTHERTX	*	=4x_DIELECTRIC	?
USB3_RX2OTHERRX	*	=4x_DIELECTRIC	?
USB3_TX2RX	*	=6x_DIELECTRIC	?
USB3_RX2TX	*	=6x_DIELECTRIC	?
USB3_2OTHERHS	*	=4x_DIELECTRIC	?
USB3_2OTHER	*	=3x_DIELECTRIC	?

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

Note: 80ohm constraints are actually 85ohm

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING			
	SPI_45S	SPI	TPAD_SPI_MOSI	15 30	TP SPI
	SPI_45S	SPI	TPAD_SPI_MISO	15 30	
	SPI_45S	SPI	TPAD_SPI_CLK	15 30	
USB_BT	USB_80D	USB	USB_BT_P	14 22	Internal USB
USB_BT	USB_80D	USB	USB_BT_N	14 22	
	USB_80D	USB	USB_BT_R_P	22	
	USB_80D	USB	USB_BT_R_N	22	
USB_BT	USB_80D	USB	USB_BT_CONN_P		
USB_BT	USB_80D	USB	USB_BT_CONN_N		
USB_TPAD	USB_80D	USB	NC_USB_TPADP	14 64	
USB_TPAD	USB_80D	USB	NC_USB_TPADN	14 64	
USB_HPM	USB_85D	USB	USB_HPM_P	28 29	I/O Port Device USB
USB_HPM	USB_85D	USB	USB_HPM_N	28 29	
	USB_85D	USB	USB_HPM_R_P	26	
	USB_85D	USB	USB_HPM_R_N	26	
	USB_80D	USB	USB_EXTA_P	14 26 64	I/O Port Host USB
	USB_80D	USB	USB_EXTA_N	14 26 64	
	USB_85D	USB	USB_EXTA_F_P	26	
	USB_85D	USB	USB_EXTA_F_N	26	
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_P	14 29 64	
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_N	14 29 64	
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_C_P		
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_C_N		
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_P	29	
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_N	29	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_P	14 29	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_N	14 29	
	USB_80D	USB3_PCH_RX	USB3_EXTD_D2R_P	14 27	I/O Port DCI
	USB_80D	USB3_PCH_RX	USB3_EXTD_D2R_N	14 27	
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_P	27 29	
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_N	27 29	
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_C_P	14 29	
	USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_C_N	14 29	
	UART_45S	UART	SMC_DEBUGPRT_TX_L	26 31 32 64	
	UART_45S	UART	SMC_DEBUGPRT_RX_L	26 31 32 64	
USB_EXTB	USB_80D	USB	NC_USB_EXTBP	14 64	USB EXTB nets (Left USB port)
USB_EXTB	USB_80D	USB	NC_USB_EXTBN	14 64	
USB_EXTB	USB_80D	USB	USB2_EXTB_F_P		
USB_EXTB	USB_80D	USB	USB2_EXTB_F_N		
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	NC_USB3_EXTB_D2RP	14 64	
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	NC_USB3_EXTB_D2RN	14 64	
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_P		
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_N		
	USB_80D	USB3_PCH_TX	NC_USB3_EXTB_R2D_CP	14 64	
	USB_80D	USB3_PCH_TX	NC_USB3_EXTB_R2D_CN	14 64	
USB_EXTC	USB_80D	USB	USB2_EXTC_P		USB EXTC nets (Left USB port)
USB_EXTC	USB_80D	USB	USB2_EXTC_N		
USB_EXTC	USB_80D	USB	USB2_EXTC_F_P		
USB_EXTC	USB_80D	USB	USB2_EXTC_F_N		
USB3_EXTC_RX	USB_80D	USB3_PCH_RX	USB3_EXTC_D2R_P		
USB3_EXTC_RX	USB_80D	USB3_PCH_RX	USB3_EXTC_D2R_N		
USB3_EXTC_TX	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_P		
USB3_EXTC_TX	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_N		
	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_C_P		
	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_C_N		
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3RPCIE_SD_D2R_P		
USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3RPCIE_SD_D2R_N		
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3RPCIE_SD_R2D_C_P		
USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3RPCIE_SD_R2D_C_N		
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P		
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_N		
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_P		
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_N		
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	14	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P		
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N		
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P		
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N		
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P		
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N		
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK		

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x_DIELECTRIC	?
CLK_LPC	*	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x_DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_ITP	*	=2:1_SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	*	=3x_DIELECTRIC	?
DP_2OTHERHS	*	=4x_DIELECTRIC	?
DP_2OTHER	*	=3x_DIELECTRIC	?
DP_AUX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2DP	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_AUX	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP_TX	DP_TX	*	DP_2DP
DP_TX	*_TX	*	DP_2OTHERHS
DP_TX	*_RX	*	DP_2OTHERHS
DP_TX	*	*	DP_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC AD<3..0>	14 31
LPC_FRAME_L	LPC_45S	LPC	LPC FRAME L	14 31
	LPC_45S	LPC	LPCPLUS RESET L	
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC CLK24M SMC	17 31
	CLK_LPC_45S	CLK_LPC	LPC CLK24M SMC R	12 17
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC CLK24M LPCPLUS	
	CLK_LPC_45S	CLK_LPC	TP_LPC CLK24M LPCPLUS R	12 62
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS PCH CLK	14 16 34
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS PCH DATA	14 16 34
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML PCH 0 CLK	14 34
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML PCH 0 DATA	14 34
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS SMC 1 S0 SCL	14 31 34 36 53 72
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS SMC 1 S0 SDA	14 31 34 36 53 72
HDA_BIT_CLK	HDA_45S	HDA	HDA BIT CLK	12 40
	HDA_45S	HDA	HDA BIT CLK R	12
HDA_SYNC	HDA_45S	HDA	HDA SYNC	12 40
	HDA_45S	HDA	HDA SYNC R	12
HDA_RST_L	HDA_45S	HDA	HDA RST R L	12
	HDA_45S	HDA	HDA RST L	12 40
HDA_SDIN0	HDA_45S	HDA	HDA SDIN0	12 40 64
HDA_SDOUT	HDA_45S	HDA	HDA SDOUT	12 40
	HDA_45S	HDA	HDA SDOUT R	12 17
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	13 32
	CLK_SLOW_45S	CLK_SLOW	SMC CLK32K	
SPI_CLK	SPI_45S	SPI	SPI CLK R	14 37
	SPI_45S	SPI	SPI CLK	37
SPI_MOSI	SPI_45S	SPI	SPI MOSI R	14 37
	SPI_45S	SPI	SPI MOSI	37
SPI_MISO	SPI_45S	SPI	SPI MISO	14 37
SPI_CS0	SPI_45S	SPI	SPI CS0 R L	14 37
	SPI_45S	SPI	SPI CS0 L	37
	SPI_45S	SPI	SPI SMC CLK	31 37
	SPI_45S	SPI	SPI SMC MOSI	31 37
	SPI_45S	SPI	SPI SMC MISO	31 37
	SPI_45S	SPI	SPI SMC CS L	31 37
	SPI_45S	SPI	SPI MLB CLK	37
	SPI_45S	SPI	SPI MLB MOSI	37
	SPI_45S	SPI	SPI MLB MISO	37
	SPI_45S	SPI	SPI MLB CS L	37
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D P	22
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D N	22
	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D C P	14 22
	PCIE_80D	PCIE_PCH_TX	PCIE AP R2D C N	14 22
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE AP D2R P	14 22
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE AP D2R N	14 22
	PCIE_80D	PCIE_PCH_RX	PCIE AP D2R C P	22
140P	PCIE_80D	PCIE_PCH_RX	PCIE AP D2R C N	22
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M AP P	12 22
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M AP N	12 22
140P	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M AP C P	22
140P	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M AP C N	22
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D P<3..0>	
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D N<3..0>	
	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D C P<3..0>	14 62
	PCIE_80D	PCIE_PCH_TX	PCIE TBT R2D C N<3..0>	14 62
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R P<3..0>	14 62
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R N<3..0>	14 62
	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R C P<3..0>	
	PCIE_80D	PCIE_PCH_RX	PCIE TBT D2R C N<3..0>	
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M TBT P	12 29 62 64
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M TBT N	12 29 62 64
XDP_TDI	PCH_45S	PCH_ITP	XDP PCH TDI	12 16
XDP_TDO	PCH_45S	PCH_ITP	XDP PCH TDO	12 16
XDP_TMS	PCH_45S	PCH_ITP	XDP PCH TMS	12 16
XDP_TCK	PCH_45S	PCH_ITP	XDP PCH TCK	12 16
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE CAMERA R2D P	24 25
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE CAMERA R2D N	24 25
	PCIE_80D	PCIE_PCH_TX	PCIE CAMERA R2D C P	14 25
	PCIE_80D	PCIE_PCH_TX	PCIE CAMERA R2D C N	14 25
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE CAMERA D2R P	14 25 64
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE CAMERA D2R N	14 25 64
	PCIE_80D	PCIE_PCH_RX	PCIE CAMERA D2R C P	24 25
	PCIE_80D	PCIE_PCH_RX	PCIE CAMERA D2R C N	24 25
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M CAMERA P	12 25
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M CAMERA N	12 25
	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M CAMERA C P	24 25
	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M CAMERA C N	24 25
180P	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M DEBUG P	
180P	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M DEBUG N	
189P	DP_80D	DP_TX	DP ML P<3..0>	
189P	DP_80D	DP_TX	DP ML N<3..0>	
189P	DP_80D	DP_TX	DP ML C P<3..0>	
189P	DP_80D	DP_TX	DP ML C N<3..0>	
189P	DP_80D	DP_TX	DP ML CONN P<3..0>	
189P	DP_80D	DP_TX	DP ML CONN N<3..0>	
189P	DP_80D	DP_AUX	DP AUX CH P	
189P	DP_80D	DP_AUX	DP AUX CH N	
189P	DP_80D	DP_AUX	DP AUX CH C P	
189P	DP_80D	DP_AUX	DP AUX CH C N	
189P	DP_80D	DP_AUX	DP AUX CH CONN P	
189P	DP_80D	DP_AUX	DP AUX CH CONN N	

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK CLK32K RTCX1	
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK CLK25M CAMERA	
	CLK_25M_45S	CLK_25M	SYSCLK CLK24M CAMERA	17 24 64
	CLK_25M_45S	CLK_25M	CLK25M CAM XTALP R	
	CLK_25M_45S	CLK_25M	CLK25M CAM XTALP	
	CLK_25M_45S	CLK_25M	CLK25M CAM XTALN	
	CLK_25M_45S	CLK_25M	CLK25M CAM CLKN	24
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK CLK25M TBT	
	CLK_25M_45S	CLK_25M	SYSCLK CLK25M TBT R	
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X1	
	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X2	
	CLK_25M_45S	CLK_25M	SYSCLK CLK25M X2 R	
	CLK_25M_45S	CLK_25M	SDCLK CLK25M X2	
	CLK_25M_45S	CLK_25M	SDCLK CLK25M X2 R	
	CLK_25M_45S	CLK_25M	SDSCLK CLK25M X1	

E85 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
E85_HS_XBAR_D2R	DP_85D	DP_TX	DP TBTSNK0 ML C P<0>	5 29
E85_HS_XBAR_D2R	DP_85D	DP_TX	DP TBTSNK0 ML C N<0>	5 29
E85_HS_XBAR_R2D	DP_85D	DP_TX	DP TBTSNK0 ML C P<1>	5 29
E85_HS_XBAR_R2D	DP_85D	DP_TX	DP TBTSNK0 ML C N<1>	5 29
E85_HS	DP_85D	DP_TX	DP TBTSNK0 ML C P<3..2>	5 29
E85_HS	DP_85D	DP_TX	DP TBTSNK0 ML C N<3..2>	5 29
	DP_85D	DP_TX	DP E85SNK ML P<3..0>	27 29
	DP_85D	DP_TX	DP E85SNK ML N<3..0>	27 29
	DP_85D	DP_TX	E85 HS DP ML0 P	27 29
	DP_85D	DP_TX	E85 HS DP ML0 N	27 29
	DP_85D	DP_TX	E85 HS DP ML1 P	27 29
	DP_85D	DP_TX	E85 HS DP ML1 N	27 29
E85_LS	E85_LS_85D	E85_LS	E85 LS P<2..1>	26 29 64
E85_LS	E85_LS_85D	E85_LS	E85 LS N<2..1>	26 29 64
	E85_LS_85D	E85_LS	E85 LS MISSION P	26
	E85_LS_85D	E85_LS	E85 LS MISSION N	26
		E85_CC	E85 CC1	29 60 64
		E85_CC	E85 CC2	29 60 64

Note: 80ohm constraints are actually 85ohm

SYNC_MASTER=DEV_MLB SYNC_DATE=04/17/2014

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PCH Constraints 2

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_70D
MEM_40S	MEM_TERM	MEM_50S

Note: changed MEM_TERM physical rule to MEM_70D from MEM_73D temporarily

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>	7 20
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>	7 20
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>	7 20
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>	7 20
MEM_A_CS0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0>	7 20
MEM_A_CS1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1>	7 20
MEM_A_ODT	MEM_40S	MEM_CTRL	MEM_A_ODT<0>	7 20 61
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>	7 20
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>	7 20
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>	7 20 61
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>	7 20 61
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM_A_DQ<7..0>	7 61
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM_A_DQ<15..8>	7 61
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM_A_DQ<23..16>	7 61
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM_A_DQ<31..24>	7 61
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM_A_DQ<39..32>	7 20 61
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM_A_DQ<47..40>	7 61
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM_A_DQ<55..48>	7 61
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM_A_DQ<63..56>	7 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>	7 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>	7 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>	7 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>	7 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>	7 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>	7 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>	7 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>	7 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>	7 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>	7 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>	7 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>	7 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>	7 20 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>	7 20 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>	7 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>	7 61
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0>	7 21 64
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0>	7 21 64
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1>	7 21
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1>	7 21
MEM_B_CS0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0>	7 21 64
MEM_B_CS1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1>	7 21 64
MEM_B_ODT	MEM_40S	MEM_CTRL	MEM_B_ODT<0>	7 21 61
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0>	7 21 64
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2>	7 21
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0>	7 21 61 64
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0>	7 21 61 64
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM_B_DQ<7..0>	7 61 64
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM_B_DQ<15..8>	7 61
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM_B_DQ<23..16>	7 61
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM_B_DQ<31..24>	7 61
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM_B_DQ<39..32>	7 21 61
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM_B_DQ<47..40>	7 61
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM_B_DQ<55..48>	7 61
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM_B_DQ<63..56>	7 61
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0>	7 61 64
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0>	7 61 64
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1>	7 61
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1>	7 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2>	7 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2>	7 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3>	7 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3>	7 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4>	7 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4>	7 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5>	7 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5>	7 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6>	7 21 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6>	7 21 61
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7>	7 61
MEM_B_DQS7	MEM_70D		MEM_B_DQS_N<7>	7 61
		MEM_PWR	PP1V2_S3	8 18 19 20 21 46 52 59 60
		MEM_PWR	PPVREF_S3_MEM_VREFCA	18 19 20 21 69
		MEM_PWR	PPVREF_S3_MEM_VREFDQ_A	18 19 20
		MEM_PWR	PPVREF_S3_MEM_VREFCA	18 19 20 21 69
		MEM_PWR	PPVREF_S3_MEM_VREFDQ_B	18 19 21

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Memory Constraints

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NAND BUS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
NAND_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
NAND_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NAND_DQS	*	0.100 MM	?
NAND_IO	*	0.100 MM	?
NAND_CMD	*	0.100 MM	?

NAND:

DQS_P/N MAX LENGTH 3"
IO<7..0> SIGNALS SHOULD MATCH +/- 50MIL FROM DQS_P/N
IO<7..0> AND ASSOCIATED DQS_P/N ROUTE ON SAME LAYER. NO MORE THAN 2 VIA TRANSITIONS.
NCE<7..0>,ALE,CLE SHOULD MATCH +/- 250MIL FROM NWE
DQS_P/N & NRE_P/N SHOULD MATCH +/- 100MIL FROM NWE

NAND NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
ANI0_IO	NAND_45S	NAND_IO	ANI0 IO<7..0>	55 58
DP_ANI0_DQS	NAND_85D	NAND_DQS	ANI0 DQS P	55 58
DP_ANI0_DQS	NAND_85D	NAND_DQS	ANI0 DQS N	55 58
DP_ANI0_NRE	NAND_85D	NAND_DQS	ANI0 NRE P	55 58
DP_ANI0_NRE	NAND_85D	NAND_DQS	ANI0 NRE N	55 58
ANI0_NWE	NAND_45S	NAND_CMD	ANI0 NWE	55 58
ANI0_NCE	NAND_45S	NAND_CMD	ANI0 NCE<3..0>	55 58
ANI0_ALE	NAND_45S	NAND_CMD	ANI0 ALE	55 58
ANI0_CLE	NAND_45S	NAND_CMD	ANI0 CLE	55 58
ANI1_IO	NAND_45S	NAND_IO	ANI1 IO<7..0>	55 58
DP_ANI1_DQS	NAND_85D	NAND_DQS	ANI1 DQS P	55 58
DP_ANI1_DQS	NAND_85D	NAND_DQS	ANI1 DQS N	55 58
DP_ANI1_NRE	NAND_85D	NAND_DQS	ANI1 NRE P	55 58
DP_ANI1_NRE	NAND_85D	NAND_DQS	ANI1 NRE N	55 58
ANI1_NWE	NAND_45S	NAND_CMD	ANI1 NWE	55 58
ANI1_NCE	NAND_45S	NAND_CMD	ANI1 NCE<3..0>	55 58
ANI1_ALE	NAND_45S	NAND_CMD	ANI1 ALE	55 58
ANI1_CLE	NAND_45S	NAND_CMD	ANI1 CLE	55 58
ANI2_IO	NAND_45S	NAND_IO	ANI2 IO<7..0>	
DP_ANI2_DQS	NAND_85D	NAND_DQS	ANI2 DQS P	
DP_ANI2_DQS	NAND_85D	NAND_DQS	ANI2 DQS N	
DP_ANI2_NRE	NAND_85D	NAND_DQS	ANI2 NRE P	
DP_ANI2_NRE	NAND_85D	NAND_DQS	ANI2 NRE N	
ANI2_NWE	NAND_45S	NAND_CMD	ANI2 NWE	
ANI2_NCE	NAND_45S	NAND_CMD	ANI2 NCE<3..0>	
ANI2_ALE	NAND_45S	NAND_CMD	ANI2 ALE	
ANI2_CLE	NAND_45S	NAND_CMD	ANI2 CLE	
ANI3_IO	NAND_45S	NAND_IO	ANI3 IO<7..0>	
DP_ANI3_DQS	NAND_85D	NAND_DQS	ANI3 DQS P	
DP_ANI3_DQS	NAND_85D	NAND_DQS	ANI3 DQS N	
DP_ANI3_NRE	NAND_85D	NAND_DQS	ANI3 NRE P	
DP_ANI3_NRE	NAND_85D	NAND_DQS	ANI3 NRE N	
ANI3_NWE	NAND_45S	NAND_CMD	ANI3 NWE	
ANI3_NCE	NAND_45S	NAND_CMD	ANI3 NCE<3..0>	
ANI3_ALE	NAND_45S	NAND_CMD	ANI3 ALE	
ANI3_CLE	NAND_45S	NAND_CMD	ANI3 CLE	

NAND NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
ANI4_IO	NAND_45S	NAND_IO	ANI4 IO<7..0>	
DP_ANI4_DQS	NAND_85D	NAND_DQS	ANI4 DQS P	
DP_ANI4_DQS	NAND_85D	NAND_DQS	ANI4 DQS N	
DP_ANI4_NRE	NAND_85D	NAND_DQS	ANI4 NRE P	
DP_ANI4_NRE	NAND_85D	NAND_DQS	ANI4 NRE N	
ANI4_NWE	NAND_45S	NAND_CMD	ANI4 NWE	
ANI4_NCE	NAND_45S	NAND_CMD	ANI4 NCE<3..0>	
ANI4_ALE	NAND_45S	NAND_CMD	ANI4 ALE	
ANI4_CLE	NAND_45S	NAND_CMD	ANI4 CLE	
ANI5_IO	NAND_45S	NAND_IO	ANI5 IO<7..0>	
DP_ANI5_DQS	NAND_85D	NAND_DQS	ANI5 DQS P	
DP_ANI5_DQS	NAND_85D	NAND_DQS	ANI5 DQS N	
DP_ANI5_NRE	NAND_85D	NAND_DQS	ANI5 NRE P	
DP_ANI5_NRE	NAND_85D	NAND_DQS	ANI5 NRE N	
ANI5_NWE	NAND_45S	NAND_CMD	ANI5 NWE	
ANI5_NCE	NAND_45S	NAND_CMD	ANI5 NCE<3..0>	
ANI5_ALE	NAND_45S	NAND_CMD	ANI5 ALE	
ANI5_CLE	NAND_45S	NAND_CMD	ANI5 CLE	
ANI6_IO	NAND_45S	NAND_IO	ANI6 IO<7..0>	55 58
DP_ANI6_DQS	NAND_85D	NAND_DQS	ANI6 DQS P	55 58
DP_ANI6_DQS	NAND_85D	NAND_DQS	ANI6 DQS N	55 58
DP_ANI6_NRE	NAND_85D	NAND_DQS	ANI6 NRE P	55 58
DP_ANI6_NRE	NAND_85D	NAND_DQS	ANI6 NRE N	55 58
ANI6_NWE	NAND_45S	NAND_CMD	ANI6 NWE	55 58
ANI6_NCE	NAND_45S	NAND_CMD	ANI6 NCE<3..0>	55 58
ANI6_ALE	NAND_45S	NAND_CMD	ANI6 ALE	55 58
ANI6_CLE	NAND_45S	NAND_CMD	ANI6 CLE	55 58
ANI7_IO	NAND_45S	NAND_IO	ANI7 IO<7..0>	55 58
DP_ANI7_DQS	NAND_85D	NAND_DQS	ANI7 DQS P	55 58
DP_ANI7_DQS	NAND_85D	NAND_DQS	ANI7 DQS N	55 58
DP_ANI7_NRE	NAND_85D	NAND_DQS	ANI7 NRE P	55 58
DP_ANI7_NRE	NAND_85D	NAND_DQS	ANI7 NRE N	55 58
ANI7_NWE	NAND_45S	NAND_CMD	ANI7 NWE	55 58
ANI7_NCE	NAND_45S	NAND_CMD	ANI7 NCE<3..0>	55 58
ANI7_ALE	NAND_45S	NAND_CMD	ANI7 ALE	55 58
ANI7_CLE	NAND_45S	NAND_CMD	ANI7 CLE	55 58

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	24 25
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	24 25
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	24 25
F10A	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	24 25 64
F10Z		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	25
F10X	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	24 25
F10W	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	24 25
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	24 25
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	24 25
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	24 25
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	24 25
F10G	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	24 25
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	24 25
F10H	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	24 25
F10J	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	24 25
F10C	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	24 25
F10D	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	24 25
F10Y	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	24 25 64
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	24 25
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	24 25
F12P	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	24 25
F12N	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	24 25
F12M		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	25 53
F12L		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	25 53
F13K	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	24 25
F13J	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	24 25
F13H		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	25 53
F13G		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	25 53
F14D			S2_MEM_PWR	PP1V35_CAM	24 25
F14E			S2_MEM_PWR	PP0V675_CAM_VREF	24 25
F14B			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	25

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	0.1 MM	=STANDARD	=STANDARD	0.1 MM	0.1 MM
2TO1_DIFFPAIR	*	=STANDARD	0.2 MM	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_0_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SCL	31 34 53
SMBUS_SMC_0_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_0_S0_SDA	31 34 53
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 31 34 36 53 68
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 31 34 36 53 68
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SCL	31 34 46 48
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SDA	31 34 46 48
SMBUS_SMC_2_S3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SCL_R	
SMBUS_SMC_2_S3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_2_G3_SDA_R	
SMBUS_SMC_3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SCL	30 31 34 40
SMBUS_SMC_3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_3_SDA	30 31 34 40
SMBUS_SMC_5_G3_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SCL	31 34 41 43
SMBUS_SMC_5_G3_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_5_G3_SDA	31 34 41 43

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSI_P	43
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSI_N	43
	1TO1_DIFFPAIR		CHGR_CSI_R_P	43
	1TO1_DIFFPAIR		CHGR_CSI_R_N	43
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSO_P	43
SENSE_DIFFPAIR	1TO1_DIFFPAIR		CHGR_CSO_N	43
	1TO1_DIFFPAIR		CHGR_CSO_R_P	43
	1TO1_DIFFPAIR		CHGR_CSO_R_N	43

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SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SENSE_1TO1_P2MM	*	=1TO1_DIFFPAIR	0.200 MM	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SENSE_1TO1_P3MM	*	=1TO1_DIFFPAIR	0.300 MM	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
THERM_1TO1_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR
SPKR_DIFFPAIR	*	=1TO1_DIFFPAIR	0.400 MM	0.100 MM	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=1:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	10000
PWR_P2MM	*	0.20 MM	10000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

RF Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
RF_50S	*	=50_OHM_SE_RF	=50_OHM_SE_RF	=50_OHM_SE_RF	=50_OHM_SE_RF	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
RF	*	0.15 MM	?

J92 MLB Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_P	35 36
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_N	35 36
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	35
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	35
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P	36
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N	36
SENSE_DIFFPAIR	SENSE_1TO1_P3MM	SENSE	ISNS_1V2_S3_P	46
SENSE_DIFFPAIR	SENSE_1TO1_P3MM	SENSE	ISNS_1V2_S3_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	49
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	49
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_SUS_P	48
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_SUS_N	48
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS1_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS1_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P	36
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N	36
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_P	
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_N	
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT1_P	39 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT1_N	39 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT2_P	39 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT2_N	39 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT1_P	38 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT1_N	38 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT2_P	38 40
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_LOUT2_N	38 40
		SB_POWER	PP3V3_S5	8 11 13 15 16 17 22 33 37 46 47 51 59 60 75
		SB_POWER	PP3V3_S0	8 11 12 13 15 17 18 23 24 29 32 33 34 35 36 40 46 47 53 60 75
		GND	GND	
	RF_50S	RF	RF_A_0_DIPLEXER	22
	RF_50S	RF	RF_A_0_MATCH	22
	RF_50S	RF	RF_G_0_DIPLEXER	22
	RF_50S	RF	RF_G_0_MATCH	22
	RF_50S	RF	RF_0_ANT	22
	RF_50S	RF	RF_0_ANT_MATCH_T	22
	RF_50S	RF	RF_A_1_DIPLEXER	22
	RF_50S	RF	RF_A_1_MATCH	22
	RF_50S	RF	RF_G_1_DIPLEXER	22
	RF_50S	RF	RF_G_1_MATCH	22
	RF_50S	RF	RF_1_ANT	22
	RF_50S	RF	RF_1_ANT_MATCH_T	22
DP_EXT_ML	DP_80D	DP_TX	DP_EXT_ML_P<1..0>	
DP_EXT_ML	DP_80D	DP_TX	DP_EXT_ML_N<1..0>	
	DP_80D	DP_TX	DP_EXT_ML_C_P<1..0>	
	DP_80D	DP_TX	DP_EXT_ML_C_N<1..0>	
USB_EXTA	USB_80D	USB	DPRUSB_EXTA_P	
USB_EXTA	USB_80D	USB	DPRUSB_EXTA_N	
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	DPRUSB3_EXTA_D2R_P	
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	DPRUSB3_EXTA_D2R_N	
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	DPRUSB3_EXTA_R2D_P	
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	DPRUSB3_EXTA_R2D_N	

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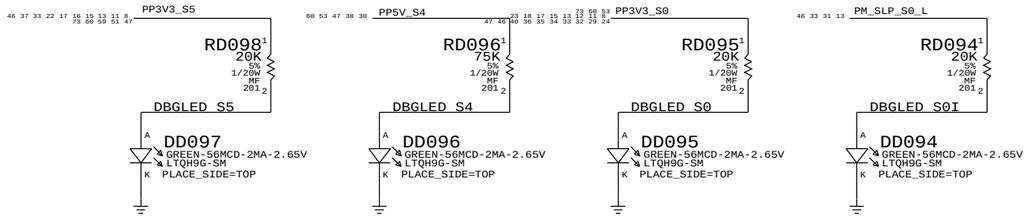
Power State Debug LEDs



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